Rockwell

RC24BKJ
V.26 bis 2400 bps Half-Duplex Modem

INTRODUCTION

The Rockwell RC24BKJ modem is a synchronous 2400 bits per second (bps) half-duplex modem in a single 68-pin plastic leaded chip carrier (PLCC) package. The RC24BKJ can operate over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The modem satisfies the telecommunication requirements specified in CCITT recommendations V.26 bis, V.26 Alternative A, V.27 ter, and V.21 Channel 2. The RC24BKJ can operate at speeds of 4800, 2400, 1200, and 300 bps, and also includes the V.27 ter short training sequence option.

The RC24BKJ is designed for use in applications that have standardized on V.26 bis for their physical layer interface. The modem's small size and low power consumption offer the user flexibility in creating a V.26 bis modem customized for specific packaging and functional requirements. Inclusion of V.27 ter and V.21 Channel 2 also provides Group 3 facsimile support for personal computers.

FEATURES

- Single 68-pin PLCC
- CCITT V.26 bis, V.26 Alternative A, V.27 ter, V.21 Channel 2
- Group 3 facsimile transmission/reception
- Low power consumption: 370 mW (typical)
- 2-wire half-duplex
- Programmable RTS-CTS turn-on time (V.26)
- Programmable RLSD turn-on and turn-off time (V.26)
- Transmit external clock capability
- Programmable dual tone generation
- Programmable tone detection
- Programmable turn-on and turn-off thresholds
- Programmable transmit output level
- Programmable interface memory interrupt
- Diagnostic capability allows telephone line quality monitoring
- Equalization
  - Automatic adaptive
  - Compromise cable (selectable)
- DTE interface: two alternate ports
  - Selectable 6500 or 8085 microprocessor bus
  - CCITT V.24 (EIA-232-D compatible)
- TTL and CMOS compatible

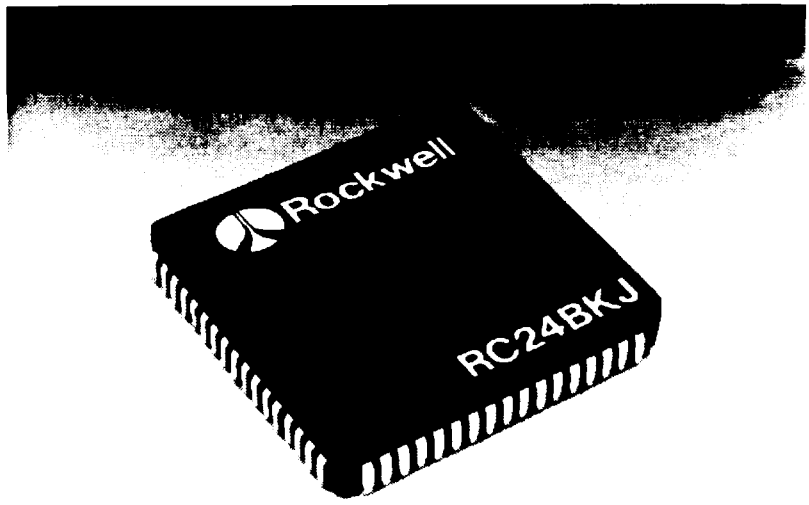


Figure 1. RC24BKJ Modem

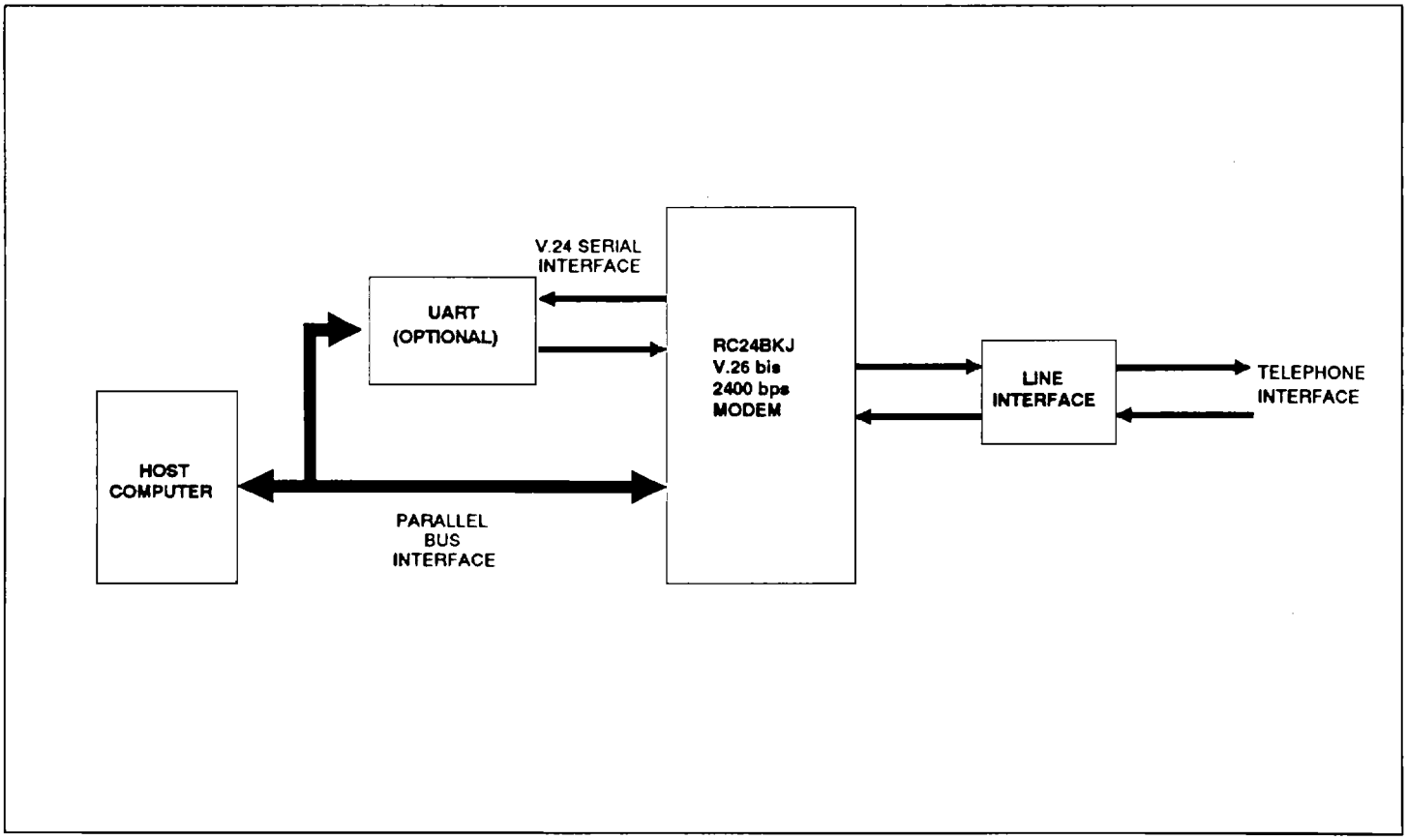


Figure 2. RC24BKJ Modem General Interface

TECHNICAL SPECIFICATIONS

Configurations, Signaling Rates and Data Rates

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

Tone Generation

The modem can generate voice-band single or dual tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. Dual tone generation allows the modem to operate as a programmable DTMF dialer.

Data Encoding

The data encoding conforms to CCITT recommendations V.26 bis, V.26 Alternative A, V.27 ter, and V.21 Channel 2.

Automatic Adaptive Equalizer

An adaptive equalizer in V.26 and V.27 ter modes compensates for transmission line amplitude and group delay distortion.

Compromise Cable Equalizers

Compromise equalization can improve performance when operating over low quality lines. The modem has cable equalizers selected by the CABLE1 and CABLE2 inputs with the characteristics shown in Table 9. The selected filter operates in both transmit and receive paths.

Transmitted Data Spectrum

The transmitted data spectrum is shaped in the baseband by an excess bandwidth finite impulse response (FIR) filter with the following characteristics:

When operating at 1600 baud, the transmitted spectrum is shaped by a square root of 50% raised cosine filter.

When operating at 1200 baud, the transmitted spectrum is shaped by a square root of 90% raised cosine filter.

The transmit spectrum characteristics assume that the cable equalizers are disabled.

The out-of-band transmitter energy levels in the 4 kHz – 50 kHz frequency range are below –55.0 dBm.

Turn-on Sequences

Transmitter turn-on sequence times are shown in Table 2.

When the modem is configured for V.26 bis or V.26 Alternative A, the turn-on sequence consists of two segments. The first segment is continuous unscrambled ones. The second segment may be either continuous unscrambled or scrambled ones depending on whether the scrambler/descrambler is selected. Scrambling in the transmitter and descrambling in the receiver, when selected, is done in accordance with CCITT V.27 ter. The duration of both segments is programmable in increments of 0.833 ms from 0 to 54.6 seconds. The default duration of each segment is 30 ms.

Turn-off Sequences

For V.26, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled or unscrambled ones.

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of remaining data and scrambled ones at 1600 baud followed by 20 ms of no transmitted energy.

In V.21, the transmitter turns off within 7 ms after $\overline{\text{RTS}}$ goes OFF.

When operating in parallel data mode, the turn-off sequence may be extended by 8 bit times.

Table 2. Turn-On Sequence Times

Configuration	$\overline{\text{RTS}}$ On to $\overline{\text{CTS}}$ On	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.26 (All speeds)	Programmable	Not Applicable
V.27 ter 4800 bps Long Train	708 ms	913 ms
V.27 ter 4800 bps Short Train	50 ms	255 ms
V.27 ter 2400 bps Long Train	943 ms	1148 ms
V.27 ter 2400 bps Short Train	67 ms	272 ms
V.21 300 bps	≤ 14 ms	≤ 14 ms

Table 1. Configurations and Rates

Configuration	Modulation*	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ± 0.01%	Baud (Symbols/Sec.)	Bits per Symbol	Constellation Points
V.26 bis 2400	DPSK	1800	2400	1200	2	4
V.26 2400 A	DPSK	1800	2400	1200	2	4
V.26 1200	DPSK	1800	1200	1200	1	2
V.27 ter 4800	DPSK	1800	4800	1600	3	8
V.27 ter 2400	DPSK	1800	2400	1200	2	4
V.21 300	FSK	1650,1850	300	300	1	–

* Modulation legend: DPSK Differential Phase Shift Keying; FSK Frequency Shift Keying

Transmit Level

The transmitter output level is programmable in the DSP RAM from 0 dBm to –15.0 dBm and is accurate to ± 1.0 dB. The modem adjusts the output level by digitally scaling the output to the transmitter's digital-to-analog converter.

Scrambler/Descrambler

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with V.27 ter. The V.27 ter scrambler/descrambler may also be enabled in V.26 modes.

Receive Dynamic Range

The receiver satisfies PSTN performance requirements for received line signal levels from 0 dBm to –43 dBm measured at the Receiver Analog Input (RXA) input. An external input buffer and filter must be supplied between RXA and RXIN.

The default values of the programmable $\overline{\text{RLSD}}$ turn-on and turn-off threshold levels are –43 dBm and –48 dBm, respectively. The $\overline{\text{RLSD}}$ threshold levels can be programmed over the following range:

Turn on: –10 dBm to –47 dBm
Turn off: –10 dBm to –52 dBm

Receiver Timing

The timing recovery circuit can track a ± 0.01% frequency error in the associated transmit timing source.

Carrier Recovery

The carrier recovery circuit can track a ± 7 Hz frequency offset in the received carrier.

Clamping

Received Data (RXD) is clamped to a constant mark whenever $\overline{\text{RLSD}}$ is off.

Tone Detectors

The tone detector signal path is separate from the main received signal path thus enabling tone detection to be independent of the receiver status. Tone detector 3 operates in all receive modes. Tone detectors 1 and 2 operate in all modes except V.27 ter. The filter coefficients of each filter are host programmable in RAM.

General Specifications

The modem power and environmental requirements are shown in Tables 3 and 4, respectively.

Table 3. Power Requirements

Voltage	Current (Typ.) @ 25°C	Current (Max.) @ 25°C
+5 VDC ± 10% – 5 VDC ± 10%	60 mA @ 5.0 V 14 mA @ 5.0 V	100 mA @ 5.0 V 25 mA @ 5.0 V
Note: Input voltage ripple ≤ 0.1 volts peak-to-peak. The amplitude of any frequency between 20 kHz and 150 kHz must be less than 500 µV peak.		

Table 4. Environmental Requirements

Parameter	Specification
Temperature	
Operating	0°C to +70°C (32°F to 158°F)
Storage	–55°C to +125°C (–67°F to 257°F)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

HARDWARE INTERFACE SIGNALS

The modem functional hardware interface signals are shown in Figure 3. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two-voltage system (e.g., 0 VDC for TTL or –12 VDC for EIA-232-D) is called active low and is represented by a small circle at the signal point. Active low signals are overscored (e.g., $\overline{POR}$).

Open-collector (open-source or open-drain) outputs are denoted by small half circle (e.g., signal $\overline{IRQ}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low, while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The modem pin assignments are shown in Figure 4. The pin assignments are listed by pin number in Table 5.

The hardware interconnect signals shown in Figure 3 are listed by functional group in Table 6. The digital and analog signal interface characteristics are defined in Tables 7 and 8, respectively. The hardware interface signals are defined in Table 9.

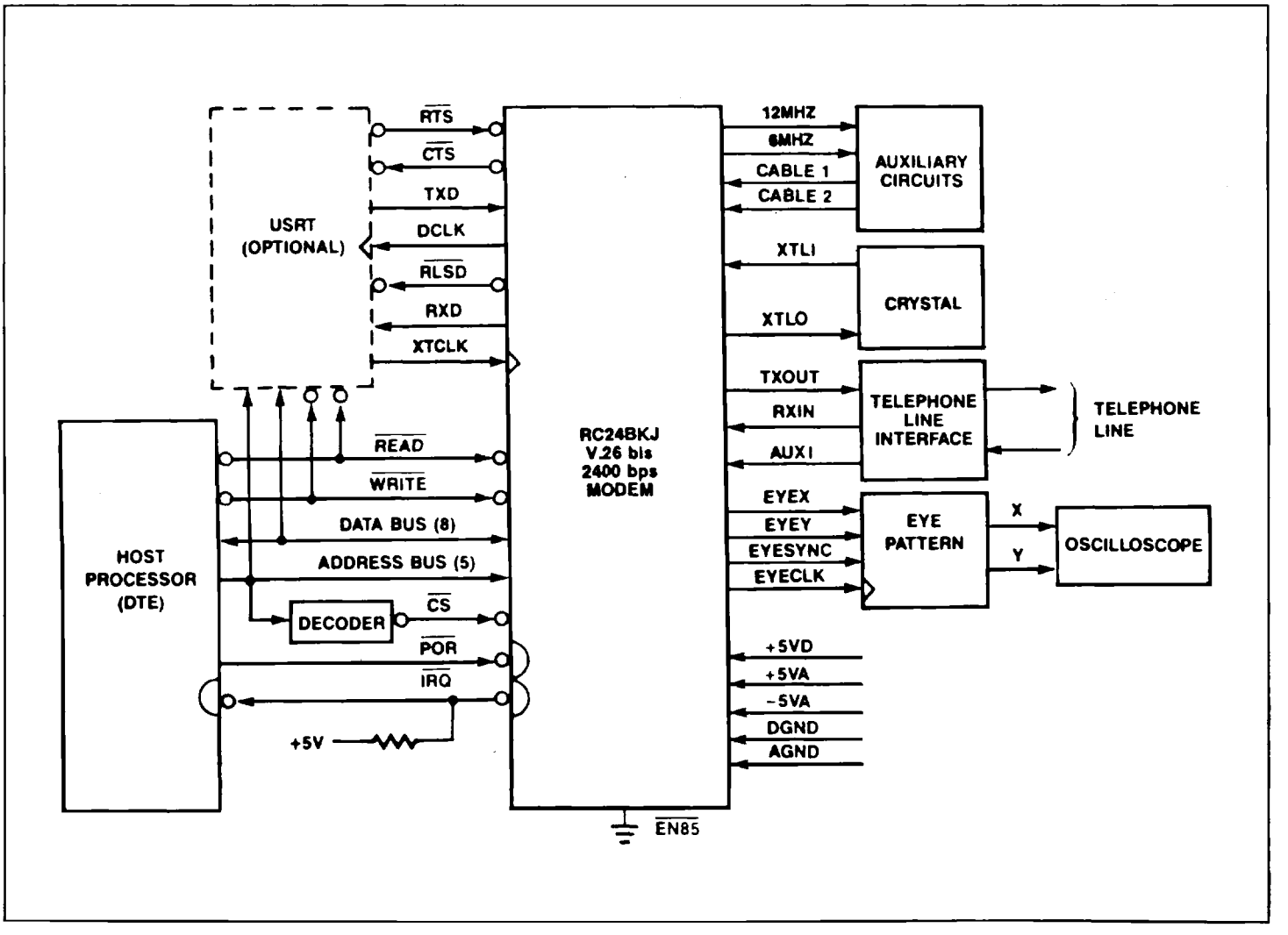


Figure 3. RC24BKJ Modem Functional Interconnect Diagram

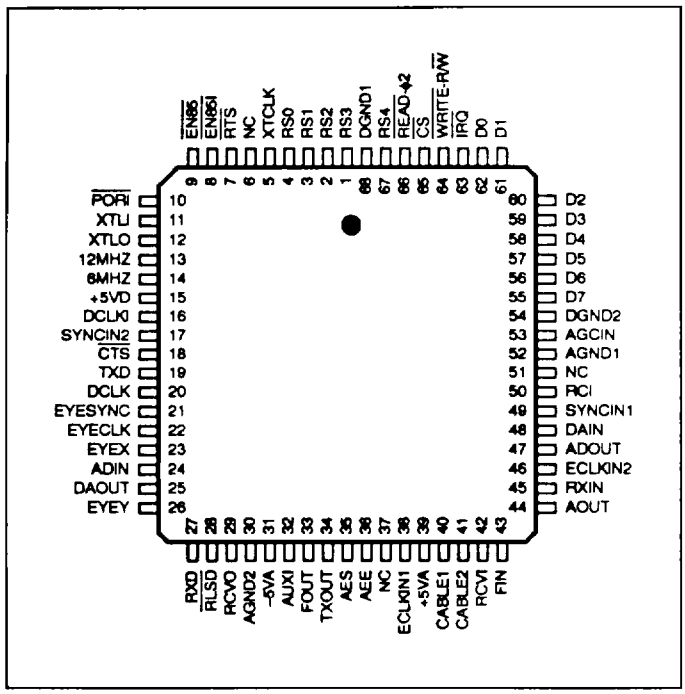


Figure 4. RC24BKJ Modem Pin Assignments

Table 5. RC24BKJ Modem Pin Assignments

Pin Number	Signal Name	I/O Type
1	RS3	IA
2	RS2	IA
3	RS1	IA
4	RS0	IA
5	XTCLK	IA
6	NC	
7	RTS	IA
8	EN85I	IA
9	EN85	R
10	PORI	ID
11	XTLI	R
12	XTLO	R
13	12MHZ	OD
14	6MHZ	OD
15	+5VD	PWR
16	DCLKI	R
17	SYNCIN2	R
18	CTS	OA
19	TXD	IA
20	DCLK	OA
21	EYESYNC	OA
22	EYECLK	OA
23	EYEX	OA
24	ADIN	R
25	DAOUT	R
26	EYEY	OA
27	RXD	OA
28	RLSD	OA
29	RCVO	R
30	AGND2	GND
31	-5VA	PWR
32	AUXI	AC
33	FOUT	R
34	TXOUT	AA
35	AES	R
36	AEE	R
37	NC	
38	ECLKIN1	R
39	+5VA	PWR
40	CABLE1	IB
41	CABLE2	IB
42	RCVI	R
43	FIN	R
44	AOUT	R
45	RXIN	AB
46	ECLKIN2	R
47	ADOUT	R
48	DAIN	R
49	SYNCIN1	R
50	RCI	R
51	NC	
52	AGND1	R
53	AGCIN	R
54	DGND2	GND
55	D7	IA/OB
56	D6	IA/OB
57	D5	IA/OB
58	D4	IA/OB
59	D3	IA/OB
60	D2	IA/OB
61	D1	IA/OB
62	D0	IA/OB
63	IRQ	OC
64	WRITE-R/W	IA
65	CS	IA
66	READ-φ2	IA
67	RS4	IA
68	DGND1	GND

Notes: 1. NC = No connection, leave pin disconnected (open).
2. I/O Type: Digital signals: see Table 7;
Analog signals: see Table 8.

Table 6. Modem Hardware Interface Signals

Name	Type[1]	Description
Overhead		
XTLI	R	Connect to Crystal/Oscillator
XTLO	R	Connect to Crystal/Oscillator
PORI	ID	Power-On-Reset Input
+5VD	PWR	Connect to Digital +5V Power
+5VA	PWR	Connect to Analog +5V Power
-5VA	PWR	Connect to Analog -5V Power
DGND1, DGND2	GND	Connect to Digital Ground
AGND1, AGND2	GND	Connect to Analog Ground
Microprocessor Interface		
D7	IA/OB	Data Bus Line 7
D6	IA/OB	Data Bus Line 6
D5	IA/OB	Data Bus Line 5
D4	IA/OB	Data Bus Line 4
D3	IA/OB	Data Bus Line 3
D2	IA/OB	Data Bus Line 2
D1	IA/OB	Data Bus Line 1
D0	IA/OB	Data Bus Line 0
RS4	IA	Register Select 4
RS3	IA	Register Select 3
RS2	IA	Register Select 2
RS1	IA	Register Select 1
RS0	IA	Register Select 0
CS	IA	Chip Select
READ-φ2	IA	Read Strobe (808X), φ2 Clock (65XX)
WRITE-R/W	IA	Write Strobe (808X), R/W (65XX)
IRQ	OC	Interrupt Request
V.24 Interface		
RTS	IA	Request to Send
CTS	OA	Clear to Send
TXD	IA	Transmit Data
RXD	OA	Received Data
RLSD	OA	Received Line Signal Detected
DCLK	OA	Transmit and Receive Data Clock
XTCLK	IA	External Transmit Data Clock
Analog Signals		
TXOUT	AA	Connect to Smoothing Filter Input
RXIN	AB	Connect to Anti-aliasing Filter Output
AUXI	AC	Auxiliary Analog Input

Table 6. Modem Hardware Interface Signals (Cont'd)

Name	Type[1]	Description
Auxiliary Circuits		
EN85	IA	Enable 8085 Bus
12MHz	OD	12 MHz Output
6MHz	OD	6 MHz Output
CABLE1	IB	Cable Equalizer Select 1
CABLE2	IB	Cable Equalizer Select 2
Serial Diagnostic Interface		
EYEX	OA	Serial Eye Pattern X Output
EYEY	OA	Serial Eye Pattern Y Output
EYECLK	OA	Serial Eye Pattern Clock
EYESYNC	OA	Serial Eye Pattern Strobe
Modem Interconnect		
DCLKI	R	Connect to DCLK
ECLKIN1	R	Connect to EYECLK
ECLKIN2	R	Connect to EYECLK
SYNCIN1	R	Connect to EYESYNC
SYNCIN2	R	Connect to EYESYNC
RCVI	R	Connect to RCVO
RCVO	R	Mode Select Output
ADIN	R	Connect to ADOUT
ADOUT	R	ADC Output
DAIN	R	Connect to DAOUT
DAOUT	R	DAC/AGC Output
EN85I	R	Connect to EN85
AEE	R	Connect to Analog Ground
AES	R	Connect to Analog Ground
AGCIN	R	AGC Input
AOUT	R	Smoothing Filter Output
FIN	R	Connect to FOUT
FOUT	R	Smoothing Filter Output
RCI	R	Connect to +5V through resistor

Notes:
1. I/O types are described in Table 7 (digital signals) and Table 8 (analog signals).
2. R = Required overhead connection; no connection to host equipment.
3. Unused inputs tied to +5V or ground require individual 10K Ω series resistors.

Table 7. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}				Vdc	
Types IA and IB		2.2	–	V_{CC}		
Type ID		0.8(V_{CC})	–	V_{CC}		
Input High Current Type IB	I_{IH}	–	–	40	µA	V_{CC} = 5.5V, V_{IN} = 5.5V
Input Low Voltage	V_{IL}	–0.3	–	0.6	Vdc	
Input Low Current Type IB	I_{IL}	–	–	–400	µA	V_{CC} = 5.5V
Input Leakage Current Types IA and ID	I_{IN}	–	–	±2.5	µA	V_{IN} = 0 to +5V, V_{CC} = 5.5V
Output High Voltage Types OA and OB	V_{OH}	3.5	–	–	Vdc	I_{LOAD} = – 100 µA
Output High Current Type OD	I_{OH}	–	–	–0.1	mA	
Output Low Voltage	V_{OL}				Vdc	
Types OA and OC		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Output Low Current Type OD	I_{OL}	–	–	100	µA	
Output Leakage Current Types OA and OB	I_{LO}	–	–	±10	µA	V_{IN} = 0.4 to V_{CC} –1
Capacitive Load	C_L				pF	
Types IA and ID		–	5	–		
Type IB		–	20	–		
Capacitive Drive	C_D				pF	
Types OA, OB, and OC		–	100	–		
Type OD		–	50	–		
Circuit Type						
Type IA						TTL
Type IB						TTL with pull-up
Type ID						POR
Types OA and OB						TTL with 3-state
Type OC and OE						Open drain
Type OD						Clock
Power Dissipation	P_D		370	625	mW	V_{CC} = 5.0 V @ 25°C

Note: Loads on 12MHz and 6MHz outputs must be balanced within 20%.

Table 8. Analog Interface Characteristics

Name	Type	Characteristic
TXOUT	AA	Maximum output: ±3.03 volts Minimum load: 10K Ω Smoothing filter transfer function: 28735.63/(s + 11547.34)
RXIN	AB	Input impedance: High impedance Anti-aliasing filter transfer function: 21551.72/(s + 11547.34)
AUXI	AC	Maximum input frequency: 4800 Hz Input Impedance: High impedance Gain to TXOUT: 0 dBm ±1 dB

Table 9. Hardware Interface Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI XTLO	I O	**Crystal In and Crystal Out.** The DSP must be connected to an external crystal circuit consisting of a 24.00014 MHz crystal and two capacitors, or a square wave generator/sine wave oscillator (see Figure 6).
$\overline{\text{PORI}}$	ID	**Power-On-Reset Input.** After power is applied to the modem, the $\overline{\text{PORI}}$ pin should be driven low for at least 3 µs. The modem then enters a power-on-reset sequence. The modem is ready to use 50 ms after the low-to-high transition of $\overline{\text{PORI}}$. The POR sequence initializes the modem interface (Figure 5) to default values.
+5VD	PWR	**+ 5V Digital Supply.** +5VD must be connected to +5V ± 10%.
+5VA	PWR	**+ 5V Analog Supply.** +5VA must be connected to +5V ± 10%.
–5VA	PWR	**–5V Analog Supply.** –5VA must be connected to –5V ± 10%.
DGND1, DGND2	GND	**Digital Ground.** DGND1 and DGND2 must be connected to digital ground.
AGND1, AGND2	GND	**Analog Ground.** AGND1 and AGND2 must be connected to analog ground.
		MICROPROCESSOR BUS Address, data, control, and interrupt hardware interface signals allow modem connection to an 8085 or 6500 bus compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors, such as the 8080 or 68000. The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits.
D0–D7	IA/OB	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable ($\overline{\text{READ}}$–ϕ2) and Write Enable ($\overline{\text{WRITE}}$–R/$\overline{\text{W}}$) signals. During a read cycle, data from the DSP interface memory register is gated onto the data bus by means of three-state drivers in the DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state. During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
RS0–RS4	IA	**Register Select Lines.** The five active high Register Select inputs (RS0–RS4) address interface memory registers within the DSP when $\overline{\text{CS}}$ is low. These lines are typically connected to address lines A0–A4. When selected by $\overline{\text{CS}}$ low, the DSP decodes RS0 through RS4 to address one of 32 8-bit internal interface memory registers (00–1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0–D7).

Table 9. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
$\overline{CS}$	IA	**Chip Select.** The active low $\overline{CS}$ input selects and enables the modem DSP for parallel data transfer between the DSP and the host over the microprocessor bus. The $\overline{CS}$ input line is typically connected to address line A5 through a decoder.
$\overline{READ}$-ϕ2 WRITE-R/$\overline{W}$	IA	**Read Enable-ϕ2** **Write Enable-R/$\overline{W}$.** When $\overline{EN85}$ is low (8085 bus selected), reading or writing is controlled by the host pulsing either $\overline{READ}$ or WRITE input low, respectively, during the microprocessor bus access cycle .
$\overline{IRQ}$	OC	**Interrupt Request.** $\overline{IRQ}$ interrupt request output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The $\overline{IRQ}$ output can be enabled in DSP interface memory to indicate immediate change of conditions in the modem. The use of $\overline{IRQ}$ is optional depending upon modem application. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). The $\overline{IRQ}$ output can be wire-ORed with other $\overline{IRQ}$ lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high). Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5V is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{IRQ}$ output is used, a resistor value of 5.6K ohms ±20%, 0.25 W, is sufficient.
		V.24 SERIAL INTERFACE Seven pins provide timing, data, and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to EIA-232-D voltage levels.
TXD	IA	**Transmit Data.** The modem obtains serial data to be transmitted from the local DTE on the Transmit Data (TXD) input in serial data mode (selected by PDM bit in interface memory), or from the interface memory Transmit Data Register (DBUFF) in parallel data mode (selected by PDM bit).
RXD	OA	**Received Data.** The modem presents received serial data to the local DTE on the Received Data (RXD) output and to the interface memory Receive Data Register (DBUFF) in both serial and parallel data modes.
$\overline{RTS}$	IA	**Request to Send.** The active low $\overline{RTS}$ input allows the modem to transmit data present at TXD in the serial data mode or in DBUFF in the parallel data mode when $\overline{CTS}$ becomes active. The $\overline{RTS}$ hardware control input is logically ORed with the RTSP bit (Table 10) by the modem to form the resultant control signal.
$\overline{CTS}$	OA	**Clear To Send.** $\overline{CTS}$ active indicates to the local DTE that the training sequence has been completed and any data present at the TXD input in the serial data mode or in DBUFF in the parallel data mode will be transmitted. $\overline{CTS}$ response times from $\overline{RTS}$ are shown in Table 2. The $\overline{CTS}$ hardware status output parallels the operation of the CTSP bit (Table 10).

Table 9. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
$\overline{\text{RLSD}}$	OA	**Received Line Signal Detector.** For V.26 modes, $\overline{\text{RLSD}}$ turns on whenever energy above the turn-on threshold is detected. The $\overline{\text{RLSD}}$ off-to-on response time is programmable, with a default time that meets the V.26 and V.26 bis requirement of 10 ± 5 ms. The $\overline{\text{RLSD}}$ on-to-off response time is also programmable, with a default time that meets the V.26 and V.26 bis requirement of 10 ± 5 ms. For V.27 ter, $\overline{\text{RLSD}}$ goes active at the end of the training sequence. If energy is above the turn-on threshold and training is not detected, the $\overline{\text{RLSD}}$ off-to-on response time is 804 baud times. The $\overline{\text{RLSD}}$ on-to-off time is 11.6 ± 5 ms. For V.21, $\overline{\text{RLSD}}$ turns on whenever energy above the turn-on threshold is detected. For all configurations the $\overline{\text{RLSD}}$ on-to-off response time ensures that all valid data bits have appeared on RXD. The $\overline{\text{RLSD}}$ programmable threshold levels default to –43 dBm for off-to-on and to –48 dBm for on-to-off. A minimum hysteresis of 2 dBm exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis are measured with a modulated signal applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than –43 dBm.
DCLK	OA	**Data Clock.** The modem outputs a single mode-dependent synchronous data clock (DCLK) for USRT timing. The DCLK frequency is 4800, 2400, 1200, or 300 Hz (± 0.01%) with a duty cycle of 50 ± 1%. (See Figure 6.) Transmit Data (TXD) must be stable during the one microsecond period immediately preceding the rising edge of DCLK and following the rising edge of DCLK.
XTCLK	IA	**External Transmit Clock.** The XTCLK input is for an External Transmit Clock provided by the local DTE. When enabled by the EXTCLK bit in interface memory, the transmitter synchronizes to the external clock. The clock supplied at XTCLK must have a frequency equal to the data signalling rate ± 0.01% with a duty cycle of 50 ± 1%. The XTCLK input is then reflected at the DCLK output. Transmit Data (TXD) must be stable for 5 μs immediately preceding the rising edge of XTCLK.
		ANCILLARY SIGNALS
$\overline{\text{EN85}}$	IA	**Enable 85.** The $\overline{\text{EN85}}$ input selects the modem microprocessor bus compatibility. When $\overline{\text{EN85}}$ is low, the modem can interface directly to an 8085 compatible microprocessor bus using $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$. When $\overline{\text{EN85}}$ is high, the modem can interface directly to a 6500 compatible microprocessor bus using ϕ2 and R/$\overline{\text{W}}$. In the 6500 configuration, the $\overline{\text{READ}}$ input becomes ϕ2 and the $\overline{\text{WRITE}}$ input becomes R/$\overline{\text{W}}$. This selection is performed only during initialization, i.e., when power is turned on or when $\overline{\text{POR}}$ is activated.
CABLE1, CABLE2	IB IB	**Cable Equalizer Select 1 and 2.** The CABLE1 and CABLE2 inputs select equalization for the following cable lengths: **Gain (dB)*** **CABLE2 / CABLE1 / Cable Length / 700 Hz / 1500 Hz / 2000 Hz / 3000 Hz** Low / Low / 0.0 km / 0.00 / 0.00 / 0.00 / 0.00 Low / High / 1.8 km / –0.99 / –0.20 / +0.15 / +1.43 High / Low / 3.6 km / –2.39 / –0.65 / +0.87 / +3.06 High / High / 7.2 km / –3.93 / –1.22 / +1.90 / +4.58 * Relative to 1700 Hz for length of 0.4 mm diameter cable. Modems may be connected by direct wiring, such as leased telephone cable or through the PSTN, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some of its route. To minimize the impact of this copper wire passband shaping, a compromise equalizer with more attenuation at the lower frequencies than at the higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion. When selected, the equalizers are inserted in the transmit path when transmitting, and in the receive path when receiving.

Table 9. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		ANALOG SIGNALS The Transmitter Analog Output (TXOUT) and Receiver Analog Input (RXIN) allow modem connection to either a leased line or the PSTN through the appropriate buffering and an audio transformer or a data access arrangement. The Auxiliary Input (AUXI) provides access to the transmitter for summing audio signals with the modem's transmitter output. The analog signal characteristics are described in Table 8.
TXOUT	AA	**Transmitter Analog Output.** TXOUT can supply a maximum of ± 3.03 volts into a load resistance of 10K ohms minimum. A 600 ohm line impedance can be matched using an external smoothing filter with a 604 ohm series resistor in its output. The smoothing filter should have a transfer function of 28735.63/(s + 11547.34).
RXIN	AB	**Receiver Analog Input.** The RXIN input is high impedance. RXIN requires an external anti-aliasing filter between the modem and the line interface, with a transfer function of 21551.72/(s + 11547.34). The maximum input level into the anti-aliasing filter should not be greater than 0 dBm. The filters required for anti-aliasing on the receiver input and the smoothing filter on the transmitter output have a single pole within the modem's passband (11,542 radians). Internal filters compensate for its presence, therefore, the pole location must not be changed. Some variation from the recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10K ohms.
AUXI	AC	**Auxiliary Analog Input.** AUXI allows access to the transmitter for the purpose of interfacing with user-provided equipment. Because this is a sampled input, any signal above 4800 Hz will cause aliasing errors. The input is high impedance and the gain to TXOUT is 0 dBm ± 1 dB.
		DIAGNOSTIC SIGNALS Four signals provide the timing necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.
EYEX, EYEY	OA OA	**Serial Eye Pattern X Output.** **Serial Eye Pattern Y Output.** The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters. EYEX and EYEY outputs are 9-bit words with their sign bits repeated. The 9-bit data words are shifted out sign bit first. EYEX and EYEY are clocked by the rising edge of EYECLK.
EYECLK	OA	**Serial Eye Pattern Clock.** EYECLK is a 230.4 kHz clock. EYECLK is a clock derived from EYECLK and EYESYNC for shifting EYEX and EYEY data into the serial-to-parallel converters.
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a 9600 Hz strobe used for loading the eye pattern D/A converters.

SOFTWARE INTERFACE

INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F (Figure 5). Each register can be read from, or written into, by both the host and the DSP.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

Table 10 defines the interface memory bits. In Table 10, interface memory bits are referred to using the format Z:Q. The register number is designated by Z (00 through 1F), and the bit number by Q (0 through 7, 0 = LSB).

DSP RAM ACCESS

The DSP contains 16-bit words of random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) parts. The host processor can read or write both the X RAM and the Y RAM.

DSP interface memory is an intermediary during data exchanges between the host and DSP RAM. The address stored in interface memory RAM address registers by the host determines the DSP RAM address for data access.

The 16-bit words are transferred between DSP RAM and DSP interface memory once each baud or sample time as selected by the BRx (x = 1 or 2) bit. The baud and data rate are determined by the selected configuration, but the sample rate is fixed at 9600 Hz for every mode.

The DSP RAM access functions, codes, and registers are identified in Table 11.

Register Function	Register Address (Hex)	Bit 7	6	5	4	3	2	1	0	Default Value (Bin)
Interrupt Handling	1F	PIA	—	—	PIE	PIREQ	—	—	SETUP	-XX0-XX0
	1E	IA2	IA1	IE2	—	BA2	IE1	—	BA1	--0X-0X-
High Speed Control	1D	—	—	—	—	—	—	—	EXTCLK	XXXXXXX0
Not Available	1C	—	—	—	—	—	—	—	—	XXXXXXXX
	1B	—	—	—	—	—	—	—	—	XXXXXXXX
	1A	—	—	—	—	—	—	—	—	XXXXXXXX
	19	—	—	—	—	—	—	—	—	XXXXXXXX
	18	—	—	—	—	—	—	—	—	XXXXXXXX
	17	—	—	—	—	—	—	—	—	XXXXXXXX
	16	—	—	—	—	—	—	—	—	XXXXXXXX
RAM Access 2 Control & Status	15	ACC2	0	0	0	0	BR2	WRT2	CR2	00000000
	14	RAM ADDRESS 2 (ADD2)								00000000
	13	X RAM DATA 2 MSB (XDAM2)								--------
	12	X RAM DATA 2 LSB (XDAL2)								--------
	11	Y RAM DATA 2 MSB (YDAM2)								--------
	10	Y RAM DATA 2 LSB (YDAL2)/DATA BUFFER (DBUFF)								--------
V.27 Scrambler Enable and High Speed Status	0F	FED		—	—	—	—	CTSP	CDET	--XXXX--
	0E	—	SCRE	—	—	—	—	—	—	X0XXXXX
	0D	RX	PNDET	—	—	—	—	—	—	--XXXXX
	0C	—	—	DATA	SCR1	PN	P2	P1	SIDLE	XX------
Programmable Interrupts	0B	ITBMSK								00000000
	0A	TRIG		ANDOR	ITADRS					00000000
High Speed Control	09	—	EQSV	EQFZ	—	—	—	—	—	X00XXXXX
Tone Detect and High Speed Control & Status	08	FR3	FR2	FR1	12TH	PNSUC	—	—	—	---0-XXX
Mode Control*	07	RTSP	TDIS	PDM	SHTR	EPT	SQEXT	T2	—	0000001X
	06	CONF								00000100
RAM Access 1 Control & Status	05	ACC1	0	0	0	0	BR1	WRT1	CR1	10000101
	04	RAM ADDRESS 1 (ADD1)								00010111
	03	X RAM DATA 1 MSB (XDAM1)								--------
	02	X RAM DATA 1 LSB (XDAL1)								--------
	01	Y RAM DATA 1 MSB (YDAM1)								--------
	00	Y RAM DATA 1 LSB (YDAL1)								--------

NOTES:
* These bits (except RTSP and TDIS) require the setting of SETUP to become active.
— This symbol in the "Bit" columns indicates that the bit is reserved for modem use only (do not alter the X value in the "Default Value" column).
- This symbol in the "Default Value " column indicates that the bit value is determined by operating conditions.

Figure 5. RC24BKJ DSP Interface Memory Map

Table 10. Modem Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
12TH	08:4	0	**Select 12th Order.** Control bit 12TH is used to enable the tone detectors to operate as one 12th order filter (using FR3) or to operate as three parallel independent 4th order filters (FR1, FR2, FR3). The 12TH bit is valid in all receive modes except V.27 (RTSP and RTS off).
ACC1	05:7	1	**RAM Access 1.** Control bit ACC1 is used to enable the modem to access the RAM associated with the address in the ADD1 and CR1 bits. WRT1 determines if a read or write is performed.
ACC2	15:7	0	**RAM Access 2.** Control bit ACC2 is used to enable the modem to access the RAM associated with the address in the ADD2 and CR2 bits. WRT2 determines if a read or write is performed.
ADD1	04:0-7	17	**RAM Address 1.** ADD1 contains the RAM address used to access the modem's Data or Coefficient RAM (depending on CR1) via the X RAM Data 1 LSB and MSB words (2:0-7 and 3:0-7) and the Y RAM Data 1 LSB and MSB words (0:0-7 and 1:0-7).
ADD2	14:0-7	00	**RAM Address 2.** ADD2 contains the RAM address used to access the modem's Data or Coefficient RAM (depending on CR2) via the X RAM Data 2 LSB and MSB words (12:0-7 and 13:0-7) and the Y RAM Data 2 LSB and MSB words (10:0-7 and 11:0-7).
ANDOR	0A:5	0	**AND/OR Bit Mask Function.** When control bit ANDOR is a 1 and the programmable interrupt is enabled (PIE bit = 1), the modem will assert IRQ if all the bits in the register specified by ITADRS and masked by ITBMSK are ones. When ANDOR is a 0 and the programmable interrupt is enabled, the modem will assert IRQ if any one of the bits in the register specified by ITADRS and masked by ITBMSK is a one.
BA1	1E:0	–	**Buffer Available 1.** Status bit BA1 is used to indicate that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 1 LSB (YDAL1) register (00:0-7). This condition can also cause IRQ to be asserted. (See IE1 and IA1.)
BA2	1E:3	–	**Buffer Available 2.** In the parallel data mode, status bit BA2 is used to indicate that the modem has read register 10:0-7 (DBUFF) when transmitting (buffer becomes empty), or it has written register 10:0-7 (DBUFF) when receiving (buffer becomes full). In the serial data mode, BA2 is used to indicate that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 2 LSB (YDAL2) register (10:0-7). These conditions can also cause IRQ to be asserted. (See IE2 and IA2.)
BR1	05:2	1	**Baud Rate 1.** Control bit BR1 is used to enable RAM access for ADD1 at the baud rate or at the sample rate .
BR2	15:2	0	**Baud Rate 2.** Control bit BR2 is used to enable RAM access for ADD2 at the baud rate or at the sample rate.
CDET	0F:0	–	**Carrier Detected.** Status bit CDET is used to indicate that the receiver has finished receiving the training sequence or has turned on due to detecting energy above threshold, and is receiving data; or the receiver is in the idle state or is in the process of training.
CONF	06:0-7	04	**Configuration.** The CONF control bits select the transmitter/receiver configuration. **CONF — Configuration** 04 — V.26 bis 2400 bps 06 — V.26 bis 1200 bps 44 — V.26 Alternative A 2400 bps 0A — V.27 ter 4800 bps 09 — V.27 ter 2400 bps 20 — V.21 Channel 2 300 bps (FSK) 80 — Transmit: Dual Tone; Receive: Tone Detector
CR1	05:0	1	**Coefficient RAM 1 Select.** Control bit CR1 is used to enable the ADD1 address to access Coefficient RAM or Data RAM.
CR2	15:0	0	**Coefficient RAM 2 Select.** Control bit CR2 is used to enable the ADD2 address to access Coefficient RAM or Data RAM.

Table 10. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
CTSP	0F:1	–	**Clear To Send Parallel.** Status bit CTSP is used to indicate to the DTE that the training sequence has been completed and any data present at TXD in serial data mode or DBUFF in parallel data mode will be transmitted. CTSP parallels the operation of the $\overline{CTS}$ pin.
DATA	0C:5	–	**Data Mode.** Status bit DATA indicates when the high speed transmitter/receiver is in the data mode.
DBUFF	10:0-7	–	**Data Buffer.** In the parallel data mode, the host obtains received data from the modem by reading a data byte from DBUFF; the host sends data to the modem to be transmitted by writing a data byte to DBUFF.
EPT	07:3	1	**Echo Protector Tone Enable.** When control bit EPT is a 1, an unmodulated carrier is transmitted for 187.5 ms followed by 20 ms of no transmitted energy prior to the transmission of the V.27 training sequence. When EPT is a 0, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the V.27 transmission of the training sequence. (See status bit P1.)
EQFZ	09:5	0	**Equalizer Freeze.** Control bit EQFZ is used to disable updating of the receiver's adaptive equalizer taps.
EQSV	09:6	0	**Equalizer Save.** Control bit EQSV is used to disable zeroing of the adaptive equalizer taps when reconfiguring the modem or when entering the training state. Adaptive equalizer taps are also not updated during training. For short train only, this bit is used in conjunction with the SHTR bit.
EXTCLK	1D:0	0	**External Clock Select.** When control bit EXTCLK is a 1 and the modem is configured as a V.26 or V.27 transmitter, the transmitter derives its timing from an external clock supplied to the hardware input XTCLK.
FED	0F:7,6	–	**Fast Energy Detector.** Status bits FED indicate the level of the received signal.
FR1	08:5		**Frequency No. 1.** Status bit FR1 indicates when energy above tone detector 1's turn-on threshold is detected. The default detection range = 2100 Hz ± 25 Hz. FR1 is valid in all receive modes except V.27 ter (RTSP and $\overline{RTS}$ off).
FR2	08:6	–	**Frequency No. 2.** Status bit FR2 indicates when energy above tone detector 2's turn-on threshold is detected. The default detection range = 1100 Hz ± 30 Hz. FR2 is valid in all receive modes except V.27 ter (RTSP and $\overline{RTS}$ off).
FR3	08:7	–	**Frequency No. 3.** Status bit FR3 indicates when energy above tone detector 3's turn-on threshold is detected, The default detection range = 400 Hz ± 15 Hz. FR3 is valid in all receive modes (RTSP and $\overline{RTS}$ off).
IA1	1E:6	–	**Interrupt Active 1.** Status bit IA1 is used to indicate that bit BA1 caused $\overline{IRQ}$ to be asserted when enabled by the IE1 bit. (See IE1 and BA1.)
IA2	1E:7	–	**Interrupt Active 2 .** Status bit IA2 is used to indicate that bit BA2 caused $\overline{IRQ}$ to be asserted when enabled by the IE2 bit. (See IE2 and BA2.)
IE1	1E:2	0	**Interrupt Enable 1.** Control bit IE1 is used to enable assertion of $\overline{IRQ}$ when BA1 is set to a 1 by the modem. (See BA1 and IA1.)
IE2	1E:5	0	**Interrupt Enable 2.** Control bit IE2 is used to enable assertion of $\overline{IRQ}$ when BA2 is set to a 1 by the modem. (See BA2 and IA2.)
ITADRS	0A:0-4	0	**Interrupt Address.** These 5 bits specify the register upon which the programmable interrupt and ITBMSK will take effect.
ITBMSK	0B:0-7	00	**Interrupt Bit Mask.** This byte performs a bit mask on the register specified in ITADRS for the programmable interrupt processing. A one in any position in ITBMSK will cause the modem to assert $\overline{IRQ}$ on the corresponding bit or bits in the register specified by ITADRS according to the ANDOR bit and the TRIG bits if PIE is set by the host and PIREQ is reset.

Table 10. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
P1	0C:1	–	**P1 Sequence.** When configured as a V.27 transmitter, status bit P1 indicates the P1 sequence is or is not being sent. When configured as a receiver, the P1 bit has no meaning.
P2	0C:2	–	**P2 Sequence.** When configured as a V.27 transmitter, status bit P2 indicates the P2 sequence is or is not being sent. When configured as a V.27 receiver, P2 indicates the search for the P2 to PN transition is or is not occurring.
PDM	07:5	0	**Parallel Data Mode.** Control bit PDM selects either parallel data mode or serial data mode. In parallel data mode, if the modem is a transmitter, data for transmission is accepted from DBUFF (10:0-7); if the modem is a receiver, the modem provides received data to DBUFF (10:0-7) and to the RXD output pin. In serial data mode, if the modem is a transmitter, data for transmission is accepted from the TXD input pin; if the modem is a receiver, the modem provides received data only to the RXD output pin.
PIA	1F:7	–	**Programmable Interrupt Active.** Status bit PIA is used to indicate that bit PIREQ caused $\overline{IRQ}$ to be asserted when enabled by the PIE bit. (See PIE and PIREQ.)
PIE	1F:4	0	**Programmable Interrupt Enable.** Control bit PIE is used to enable assertion of $\overline{IRQ}$ when PIREQ is set to a 1 by the modem. (See PIA and PIREQ.)
PIREQ	1F:3	–	**Programmable Interrupt Request.** Status bit PIREQ is used to indicate that the interrupt condition specified by ITBMSK, ITADRS, TRIG, and ANDOR is true. (See PIA and PIE.)
PN	0C:3	–	**PN Sequence.** When the modem is configured as a V.27 transmitter, status bit PN indicates the PN sequence is or is not being sent. When the modem is configured as a V.27 receiver, PN indicates the PN sequence is or is not being received. When the modem is configured as a V.26 transmitter, status bit PN = 1 indicates that the transmitter is sending segment 1 of the synchronizing sequence (unscrambled ones). When the modem is configured as a V.26 receiver, the PN bit has no meaning.
PNDET	0D:6	–	**PN Detected.** Status bit PNDET indicates that the receiver has detected the PN portion of the training sequence or that PN has not been detected.
PNSUC	08:3	–	**PN Success.** Status bit PNSUC indicates that the receiver has successfully trained at the end of the PN portion of the V.27 training sequence or that a successful training has not occurred.
RTSP	07:7	0	**Request To Send Parallel.** Control bit RTSP is used to enable a transmit sequence. The modem will continue to transmit until RTSP is reset (or $\overline{RTS}$ is turned off) and the turn-off sequence has been completed. RTSP parallels the operation of the $\overline{RTS}$ hardware input pin. These inputs are "ORed" by the modem.
RX	0D:7	–	**Receive State.** Status bit RX indicates that the modem is in the receive or transmit state. (See RTSP.)
SCR1	0C:4	–	**Scrambled Ones.** When the modem is configured as a V.27 transmitter, status bit SCR1 indicates that scrambled ones are or are not being sent. When the modem is configured as a V.27 receiver, SCR1 indicates scrambled ones are or are not being received. When the modem is configured as a V.26 transmitter, status bit SCR1 = 1 indicates that the transmitter is sending segment 2 of the synchronizing sequence (unscrambled or scrambled ones). When the modem is configured as a V.26 receiver, status bit SCR1 = 1 indicates that the modem has detected energy above the RLSD turn-on threshold, completed AGC stabilization, and is active prior to turning on RLSD. SCR1 is reset to 0 when the receiver enters data mode and turns on RLSD, or if energy falls below the RLSD turn-off threshold before entering data mode.
SCRE	0E:6	0	**Scrambler/Descrambler Enable.** When control bit SCRE is a 1 and the modem is configured for a V.26 mode transmitter, a V.27 ter scrambler is inserted in the transmit data path. When control bit SCRE is a 1 and the modem is configured for a V.26 mode receiver, a V.27 ter descrambler is inserted in the receive data path. This bit is automatically set to a 0 by the modem when a V.26 mode is selected, and set to a 1 when a V.27 mode is selected.

Table 10. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
SETUP	1F:0	0	**Setup.** Control bit SETUP is used to inform the modem to implement a configuration change after the host writes a configuration code into the CONF bits (6:0-7) or changes any of bits 0 through 5 in register 7 (7:0-5).
SHTR	07:4	0	**Short Train Mode.** Control bit SHTR is used to enable short training sequence in valid modes.
SIDLE	0C:0	–	**Silence/Idle.** When configured as a high speed transmitter, status bit SIDLE indicates the modem is or is not transmitting silence. When configured as a high speed receiver, SIDLE indicates the modem is waiting for energy or is idling.
SQEXT	07:2	0	**Squelch Extend.** Control bit SQEXT determines the length of time (20 ms or 140 ms) in V.27 modes that the modem receiver is inhibited from receiving any signal after transmitter turn-off.
T2	07:1	1	**T/2 Equalizer Select.** When control bit T2 is a 1, the receiver's adaptive equalizer is fractionally spaced. When T2 is a 0, the equalizer is T spaced (T=1 baud time). In V.26 modes it is recommended that T2 is always set to 1; if set to 0, the receiver may not meet all specifications and performance requirements.
TDIS	07:6	0	**Training Disable.** Control bit TDIS, valid in V.27 modes only, is used to prevent the modem from recognizing a training sequence and entering the training state when receiving; or to disable sending of the training sequence when transmitting.
TRIG	0A:6-7	0	**Interrupt Triggering.** These two bits select how the programmable interrupt is to occur if this interrupt is enabled (PIE bit = 1). The host has the option to be continuously interrupted whenever the interrupt condition is true (DC level triggered), or to be interrupted only when the interrupt condition transitions from false to true, transitions from true to false, or transitions from false to true or from true to false.
WRT1	05:1	0	**RAM Write 1.** Control bit WRT1 enables the modem to write the data from the Y RAM Data 1 registers into its internal RAM or to read data from its internal RAM and store the data into the X RAM Data 1 registers and Y RAM Data 1 registers as addressed by ADD1 and CR1, and controlled by ACC1.
WRT2	15:1	0	**RAM Write 2.** Control bit WRT2 enables the modem to write the data from the Y RAM Data 2 registers into its internal RAM or to read data from its internal RAM and store the data into the X RAM Data 2 registers and Y RAM Data 2 registers as addressed by ADD2 and CR2, and controlled by ACC2.
XDAL1	02:0-7	–	**X RAM Data 1 LSB.** XDAL1 is the least significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAL2	12:0-7	–	**X RAM Data 2 LSB.** XDAL2 is the least significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
XDAM1	03:0-7	–	**X RAM Data 1 MSB.** XDAM1 is the most significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAM2	13:0-7	–	**X RAM Data 2 MSB.** XDAM2 is the most significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
YDAL1	00:0-7	–	**Y RAM Data 1 LSB.** YDAL1 is the least significant byte of the 16-bit Y RAM 1 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
YDAL2	10:0-7	–	**Y RAM Data 2 LSB.** YDAL2 is the least significant byte of the 16-bit Y RAM 2 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
YDAM1	01:0-7	–	**Y RAM Data 1 MSB.** YDAM1 is the most significant byte of the 16-bit Y RAM 1 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
YDAM2	11:0-7	–	**Y RAM Data 2 MSB.** YDAM2 is the most significant byte of the 16-bit Y RAM 2 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.

Table 11. Modem DSP RAM Access Codes

No.	Function	BRx	CRx	ADDx	Read Reg. No.
1	Received Signal Samples	0	0	15	2,3
2	Average Power	0	0	14	2,3
3	AGC Gain Word	0	1	15	2,3
4	AGC Slew Rate	0	0	95	0,1
5	Tone 1 Frequency	0	1	21	2,3
6	Tone 1 Transmit Output Level	0	0	22	2,3
7	Tone 2 Frequency	0	1	22	2,3
8	Tone 2 Transmit Output Level	0	0	23	2,3
9	Output Level	0	0	21	2,3
10	Output Level Scale Factor	0	0	20	2,3
11	Equalizer Tap Coefficients (V.26)	1	1	3A - 49	0,1, 2,3
12	Equalizer Tap Coefficients (V.27)	1	1	3A - 61	0,1, 2,3
13	Rotated Equalizer Output (Eye Pattern)	1	1	17	0,1, 2,3
14	Decision Points (Ideal)	1	0	17	0,1, 2,3
15	Error Vector	1	1	1D	0,1, 2,3
16	Rotation Angle	1	1	0C	0,1
17	Frequency Correction	1	1	18	2,3
18	Eye Quality Monitor (EQM)	1	1	0D	2,3
19	RLSD Turn-on Threshold (Receiver Sensitivity - MAXG)	0	1	24	2,3
20	RLSD Hysteresis	0	1	B7	0,1
21	V.26 Synchronizing Sequence, Segment 1 Duration	0	1	83	0,1
22	V.26 Synchronizing Sequence, Segment 2 Duration	0	1	04	2,3
23	V.26 Turn-off Sequence Duration	0	1	10	2,3
24	V.26 RLSD Off-to-On Time	0	1	03	2,3
25	V.26 RLSD On-to-Off Time	0	1	82	0,1
26	FR1 Tone Detector Coefficients (except V.26 modes)	0	1	25-2A	2,3
		0	1	A5-AA	0,1
27	FR2 Tone Detector Coefficients (except V.26 modes)	0	1	2B-30	2,3
		0	1	AB-B0	0,1
28	FR3 Tone Detector Coefficients (except V.26 modes)	0	1	31-36	2,3
		0	1	B1-B6	0,1
29	FR1 Tone Detector Coefficients (V.26 modes)	0	1	4C-51	2,3
		0	1	CC-D1	0,1
30	FR2 Tone Detector Coefficients (V.26 modes)	0	1	52-57	2,3
		0	1	D2-D7	0,1
31	FR3 Tone Detector Coefficients (V.26 modes)	0	1	58-5D	2,3
		0	1	D8-DD	0,1

MODEM INTERFACE CIRCUIT

CIRCUIT AND COMPONENTS

The modem is supplied as a 68-pin PLCC device to be designed into OEM circuit boards. The recommended modem interface circuit (Figure 6) illustrates the connections and components required to connect the modem to the OEM electronics.

If the AUXI input is not used, resistors R10 and R16 can be eliminated and AUXI must be connected to AGND2.

When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3K ohm series resistor should be used on each input (CABLE1 and CABLE2) for isolation.

Resistors R7 and R17 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dBm, the 1% resistor values shown are correct for more than 99.8% of the units.

Table 12. Typical Modem Interface Parts List

Component Designation	Component Value	Manufacturer's Part Number	Suggested Manufacturer
C11, C13	1000 pF ±5%, 50V	C124C102J5G5CA	Kemet
C7, C8, C12, C14	0.1 µF ±20%, 50V	592CX7R104M050B	Sprague
C4, C6	0.33 µF ±20%, 50V		
C9	0.01 µF ±5%, 50V		
C10	1.0 µF ±20%, 50V	SMC50T1R0M5X12	United Chem-con
C5	10.0 µF ±10%, 25V	ECEBEF100	Panasonic
C2	18 pF ±5%, 50V		
C3	39 pF ±5%, 50V		
R4	3 Ω ± 5%, 1/4W	43CX3R000J	Mepco Electra
R12	255 Ω ±1%, 1/4W		
R10, R16	1 KΩ±5%, 1/4W	5043CX1K00J	Mepco Electra
R6	3 KΩ ±5%, 1/4W	5043CX3K00J	Mepco Electra
R18, R19	10 KΩ ±1%, 1/4W		
	R7	34.8 KΩ ±1%, 1/4W	
R17	46.4 KΩ ±1%, 1/4W	CRB1/4XF46K4	R–Ohm
R11	36.5 KΩ ±1%, 1/4W	CRB1/4XF36K5	R-Ohm
R14, R15	86.6 KΩ ±1%, 1/4W	CML 1/10 T86.6 KΩ ±1%	Dale Electronics
R5	2.7 MΩ ± 5%, 1/4W	5043CX2M700J	Mepco Eletra
CR1	–5.1V ± 1%, regulator	1N4625D	Motorola
Y1	24.00014 MHz		
Y2*	24.00014 MHz		Toyocom

* A sine wave oscillator may alternatively be used (see Note 3 in Figure 6).

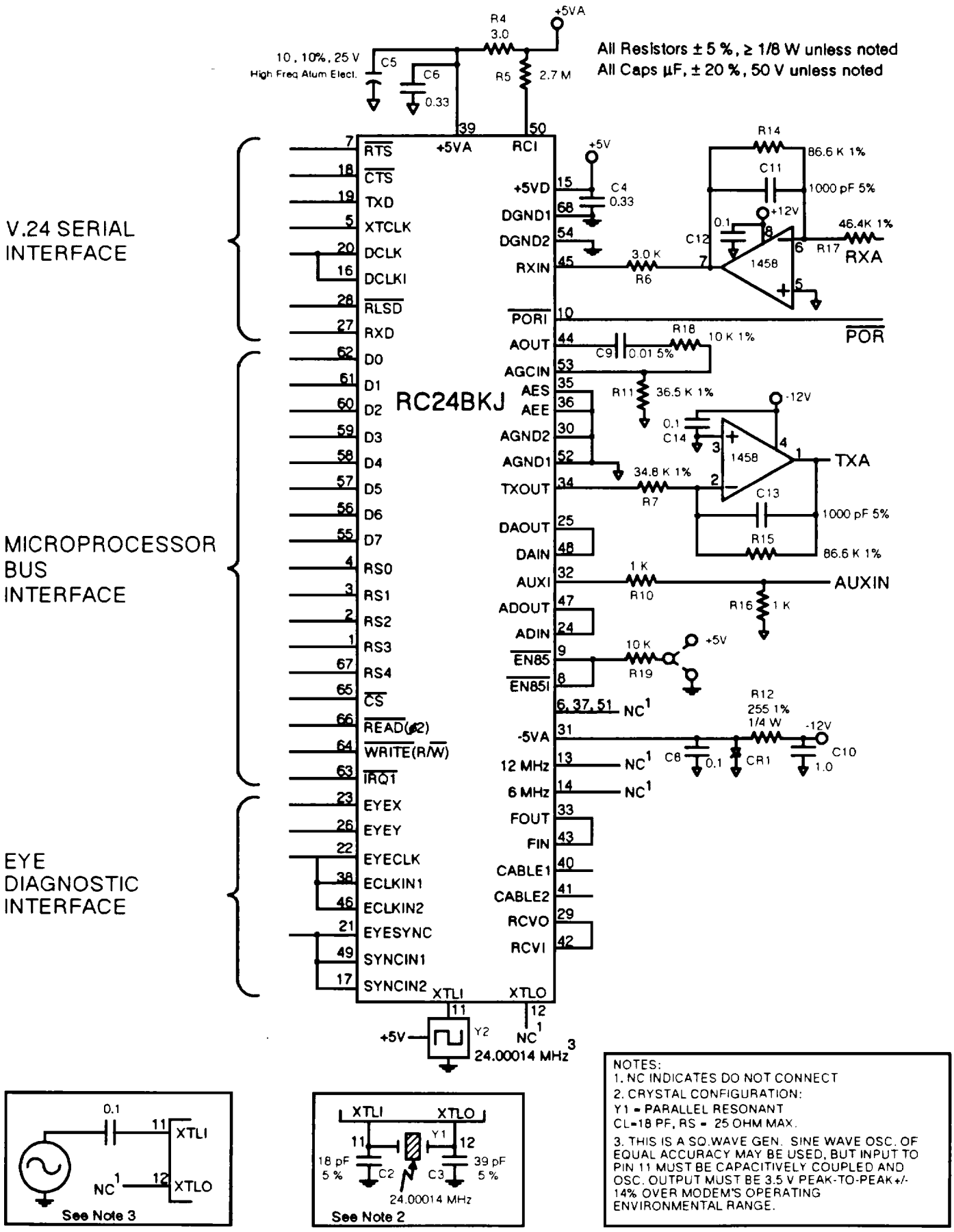
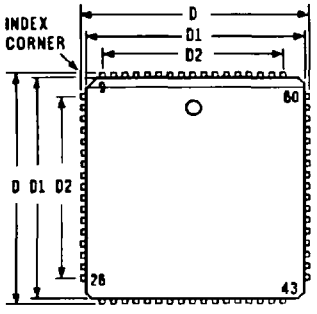
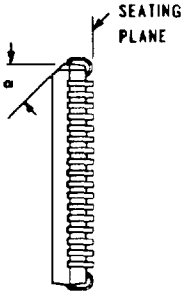


Figure 6. Recommended Modem Interface Circuit

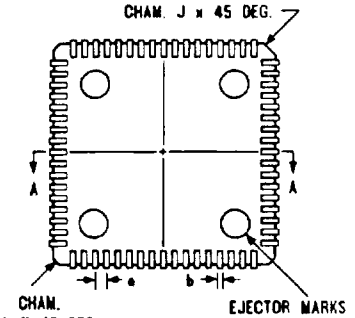
PACKAGE DIMENSIONS



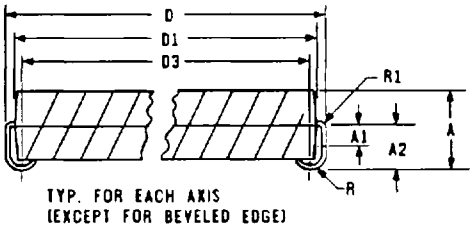
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SECTION A-A

Dim.	Millimeters Min.	Max.	Inches Min.	Max.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	25.02	25.27	0.985	0.995
D1	24.00	24.26	0.945	0.955
D2	20.19	20.45	0.795	0.805
D3	23.24	23.50	0.915	0.925
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	
Ref: PD68J/GP00-D164				

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