ispLSI® and *pLSI*® *2032*
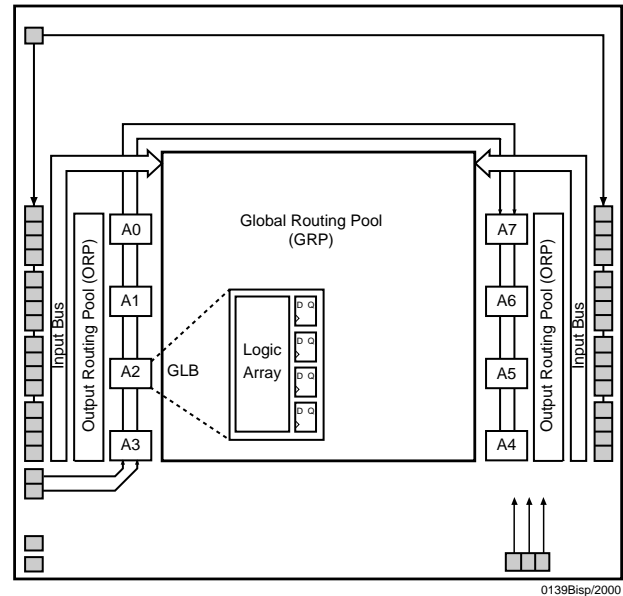
High Density Programmable Logic

Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **1000 PLD Gates**
  - **32 I/O Pins, Two Dedicated Inputs**
  - **32 Registers**
  - **High Speed Global Interconnect**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **$f$max = 180 MHz Maximum Operating Frequency**
  - **$t$pd = 5.0 ns Propagation Delay**
  - **TTL Compatible Inputs and Outputs**
  - **Electrically Erasable and Reprogrammable**
  - **Non-Volatile**
  - **100% Tested at Time of Manufacture**
  - **Unused Product Term Shutdown Saves Power**

- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **In-System Programmable (ISP™) 5-Volt Only**
  - **Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **Reprogram Soldered Devices for Faster Prototyping**

- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **Enhanced Pin Locking Capability**
  - **Three Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**

- **ispLSI DEVELOPMENT TOOLS**
  ispVHDL™ Systems
  - **VHDL/Verilog-HDL/Schematic Design Options**
  - **Functional/Timing/VHDL Simulation Options**
  ispDS™ Software
  - **Lattice HDL or Boolean Logic Entry**
  - **Functional Simulator and Waveform Viewer**
  ispDS+™ HDL Synthesis-Optimized Logic Fitter
  - **Supports Leading Third-Party Design Environments for Schematic Capture, Synthesis and Timing Simulation**
  - **Static Timing Analyzer**
  ISP Daisy Chain Download Software
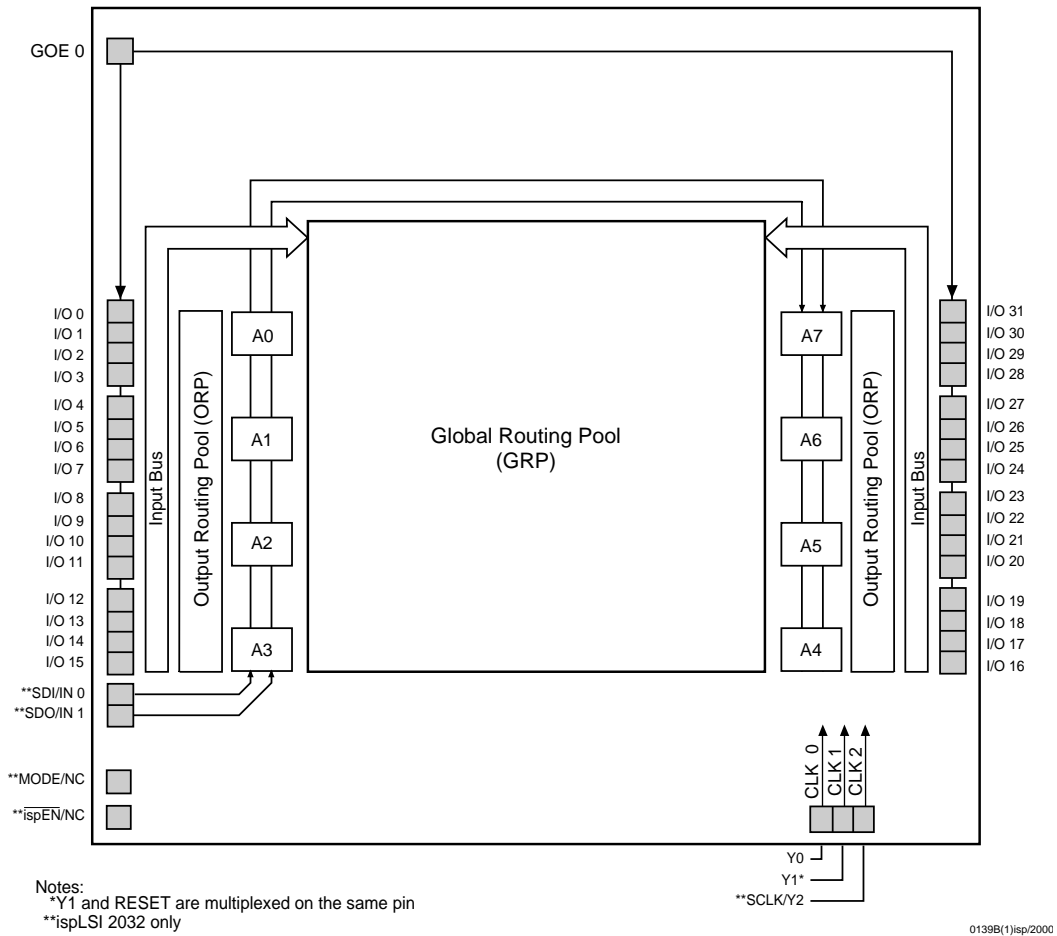
Functional Block Diagram

0139Bisp/2000

Description

The ispLSI and pLSI 2032 are High Density Programmable Logic Devices. The devices contain 32 Registers, 32 Universal I/O pins, two Dedicated Input Pins, three Dedicated Clock Input Pins, one dedicated Global OE input pin and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2032 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 2032 offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 2032 device, but multiplexes four input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 2032 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. A7 (see Figure 1). There are a total of eight GLBs in the ispLSI and pLSI 2032 devices. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

2032_03

Functional Block Diagram

Figure 1. ispLSI and pLSI 2032 Functional Block Diagram

Notes:
  *Y1 and RESET are multiplexed on the same pin
  **ispLSI 2032 only

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The devices also have 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the ORP. Each ispLSI and pLSI 2032 device contains one Megablock.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 2032 devices are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ....-0.5 to +7.0V

Input Voltage Applied .... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature .... -65 to 150°C

Case Temp. with Power Applied .... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	4.75	5.25	V
		Industrial	T_A = -40°C to + 85°C	4.5	5.5	V
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V

Table 2 - 0005/2032

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	6	pf	V_{CC} = 5.0V, V_{IN} = 2.0V
C_2	I/O Capacitance	7	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_3	Clock Capacitance	10	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2-0006/2032

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2-0008A-isp

Switching Test Conditions

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Time 10% to 90%	-135, -150, -180	≤ 1.5 ns
	-80, -110	≤ 3 ns
Input Timing Reference Levels	1.5V	
Ouput Timing Reference Levels	1.5V	
Output Load	See figure 2	

Table 2-0003/2032

3-state levels are measured 0.5V from steady-state active level.
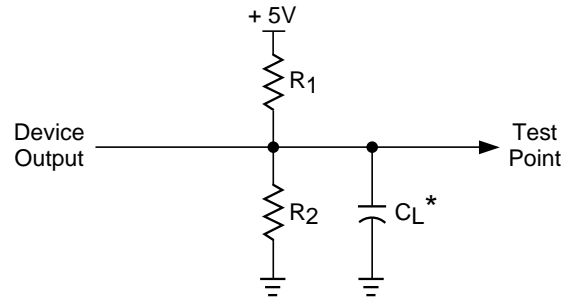
Figure 2. Test Load

*C_L includes Test Fixture and Probe Capacitance.

0213A

Output Load Conditions (see figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION			MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 8 mA			–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA			2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$ (Max.)			–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$			–	–	10	μA
I_{IL-isp}	$\overline{ispEN}$ Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$			–	–	-150	μA
I_{IL-PU}	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$			–	–	-150	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= 5V, V_{OUT} = 0.5V			–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL}= 0.0V, V_{IH}= 3.0V f_{TOGGLE} = 1 MHz	Comm.	-180, -150	–	60	–	mA
				Others	–	40	–	mA
			Industrial		–	40	–	mA

Table 2-0007/2032

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using two 16-bit counters.
3. Typical values are at V_{CC}= 5V and T_A= 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[4] COND.	#[2]	DESCRIPTION[1]	-180 MIN.	-180 MAX.	-150 MIN.	-150 MAX.	-135 MIN.	-135 MAX.	UNITS
t_{pd1}	A	1	Data Prop. Delay, 4PT Bypass, ORP Bypass	–	5.0	–	5.5	–	7.5	ns
t_{pd2}	A	2	Data Prop. Delay	–	7.5	–	8.0	–	10.0	ns
f_{max}	A	3	Clk Frequency with Internal Feedback [3]	180	–	154	–	137	–	MHz
f_{max} (Ext.)	–	4	Clk Frequency with Ext. Feedback $\left(\frac{1}{t_{su2}+t_{co1}}\right)$	125	–	111	–	100	–	MHz
f_{max} (Tog.)	–	5	Clk Frequency, Max. Toggle	200	–	167	–	167	–	MHz
t_{su1}	–	6	GLB Reg Setup Time before Clk, 4 PT Bypass	3.0	–	3.0	–	4.0	–	ns
t_{co1}	A	7	GLB Reg. Clk to Output Delay, ORP Bypass	–	4.0	–	4.5	–	4.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clk, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clk	4.0	–	4.5	–	5.5	–	ns
t_{co2}	–	10	GLB Reg. Clk to Output Delay	–	4.5	–	5.0	–	5.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clk	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	7.0	–	8.0	–	10.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	4.0	–	4.5	–	5.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	10.0	–	11.0	–	12.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	10.0	–	11.0	–	12.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	5.0	–	5.0	–	6.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	5.0	–	5.0	–	6.0	ns
t_{wh}	–	18	Ext. Synchronous Clk Pulse Duration, High	2.5	–	3.0	–	3.0	–	ns
t_{wl}	–	19	Ext. Synchronous Clk Pulse Duration, Low	2.5	–	3.0	–	3.0	–	ns

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Table 2-0030B-180/2032

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[4] COND.	#[2]	DESCRIPTION[1]	-110 MIN.	-110 MAX.	-80 MIN.	-80 MAX.	UNITS
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	13.0	–	18.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	111	–	84.0	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	77.0	–	57.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	125	–	83.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	5.5	–	7.5	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	5.5	–	8.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	7.5	–	9.5	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	6.5	–	9.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	13.5	–	19.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	6.5	–	10.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	14.5	–	24.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	14.5	–	24.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	7.0	–	12.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	7.0	–	12.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	4.0	–	6.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	4.0	–	6.0	–	ns

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Table 2-0030B-110/2032

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-180		-150		-135		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{io}	20	Input Buffer Delay	–	0.6	–	0.6	–	1.1	ns
t_{din}	21	Dedicated Input Delay	–	1.1	–	1.3	–	2.4	ns
GRP									
t_{grp}	22	GRP Delay	–	0.7	–	0.7	–	1.3	ns
GLB									
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	–	2.3	–	2.6	–	3.6	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	–	3.1	–	3.1	–	3.6	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	3.6	–	4.3	–	5.0	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	4.1	–	4.6	–	5.1	ns
t_{xoradj}	27	XOR Adjacent Path Delay [3]	–	4.8	–	5.0	–	5.6	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.2	–	0.0	–	0.0	ns
t_{gsu}	29	GLB Register Setup Time before Clock	0.5	–	0.7	–	0.3	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	1.8	–	1.8	–	3.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.7	–	0.8	–	0.7	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.0	–	1.2	–	1.1	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	2.8	–	2.9	–	4.4	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	5.9	–	6.9	–	6.4	ns
t_{ptck}	35	GLB Product Term Clock Delay	2.5	3.8	2.5	4.1	2.9	5.2	ns
ORP									
t_{orp}	36	ORP Delay	–	0.7	–	0.8	–	1.3	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.2	–	0.3	–	0.3	ns
Outputs									
t_{ob}	38	Output Buffer Delay	–	1.2	–	1.3	–	1.2	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	10.0	–	10.0	–	10.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	2.8	–	2.8	–	3.2	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	2.8	–	2.8	–	3.2	ns
t_{goe}	42	Global Output Enable	–	2.2	–	2.2	–	2.8	ns
Clocks									
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	1.9	1.9	2.1	2.1	2.3	2.3	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	1.9	1.9	2.1	2.1	2.3	2.3	ns
Global Reset									
t_{gr}	45	Global Reset to GLB	–	4.1	–	4.7	–	6.4	ns

Table 2-0036C-180/2032

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-110		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	20	Input Buffer Delay	–	1.7	–	2.2	ns
t_{din}	21	Dedicated Input Delay	–	3.4	–	4.8	ns
GRP							
t_{grp}	22	GRP Delay	–	1.7	–	2.6	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	–	4.9	–	7.2	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	–	4.8	–	7.2	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	6.2	–	8.8	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	6.8	–	9.2	ns
t_{xoradj}	27	XOR Adjacent Path Delay [3]	–	7.5	–	10.2	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.1	–	0.0	ns
t_{gsu}	29	GLB Register Setup Time befor Clock	0.5	–	0.1	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	4.0	–	6.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.6	–	0.4	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.8	–	2.2	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	5.9	–	8.8	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	7.1	–	12.8	ns
t_{ptck}	35	GLB Product Term Clock Delay	4.0	7.0	5.5	9.5	ns
ORP							
t_{orp}	36	ORP Delay	–	1.5	–	2.1	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.5	–	0.6	ns
Outputs							
t_{ob}	38	Output Buffer Delay	–	1.2	–	2.4	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	10.0	–	10.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	4.0	–	6.4	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	4.0	–	6.4	ns
t_{goe}	42	Global Output Enable	–	3.0	–	5.6	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	3.2	3.2	4.6	4.6	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.2	3.2	4.6	4.6	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	–	9.0	–	12.8	ns

Table 2-0036C-110/2032

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

ispLSI and pLSI 2032 Timing Model

0491/2032
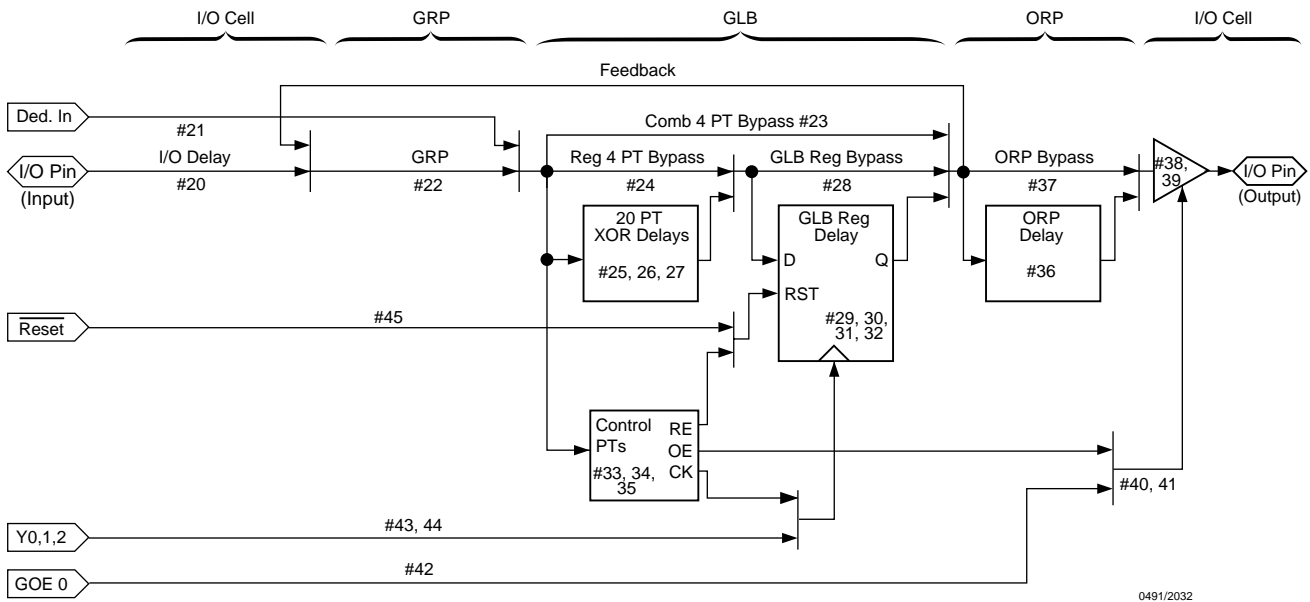
Derivations of t_{su}, t_h and t_{co} from the Product Term Clock[1]

t_{su} = Logic + Reg su - Clock (min)
= (t_{io} + t_{grp} + $t_{20ptxor}$) + (t_{gsu}) - (t_{io} + t_{grp} + $t_{ptck(min)}$)
= (#20+ #22+ #26) + (#29) - (#20+ #22+ #35)
2.1 ns = (0.6 + 0.7 + 4.1) + (0.5) - (0.6 + 0.7 + 2.5)

t_h = Clock (max) + Reg h - Logic
= (t_{io} + t_{grp} + $t_{ptck(max)}$) + (t_{gh}) - (t_{io} + t_{grp} + $t_{20ptxor}$)
= (#20+ #22+ #35) + (#30) - (#20+ #22+ #26)
1.5 ns = (0.6 + 0.7 + 3.8) + (1.8) - (0.6 + 0.7 + 4.1)

t_{co} = Clock (max) + Reg co + Output
= (t_{io} + t_{grp} + $t_{ptck(max)}$) + (t_{gco}) + (t_{orp} + t_{ob})
= (#20+ #22+ #35) + (#31) + (#36 + #38)
7.7 ns = (0.6 + 0.7 + 3.8) + (0.7) + (0.7 + 1.2)

Note: Calculations are based upon timing specifications for the ispLSI and pLSI 2032-180L

Table 2- 0042-16/2032

9

Power Consumption

Power Consumption in the ispLSI and pLSI 2032 device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax
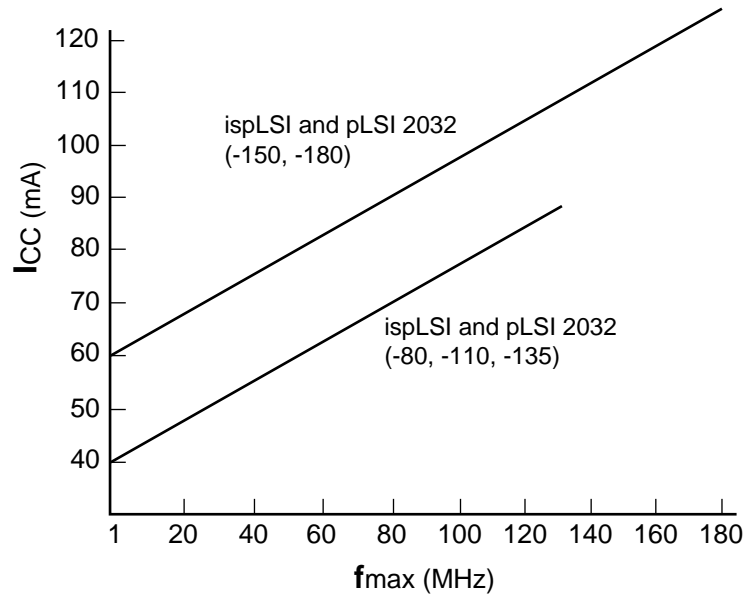
Notes: Configuration of Two 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI and pLSI 2032 using the following equation:

For 2032 -150, -180: $I_{CC}(mA) = 30 + (\# \text{ of PTs} * 0.46) + (\# \text{ of nets} * \text{Max freq} * 0.012)$
For 2032 -135, -110, -80: $I_{CC}(mA) = 21 + (\# \text{ of PTs} * 0.30) + (\# \text{ of nets} * \text{Max freq} * 0.012)$

Where:
   # of PTs = Number of Product Terms used in design
   # of nets = Number of Signals used in device
   Max freq = Highest Clock Frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A/2032
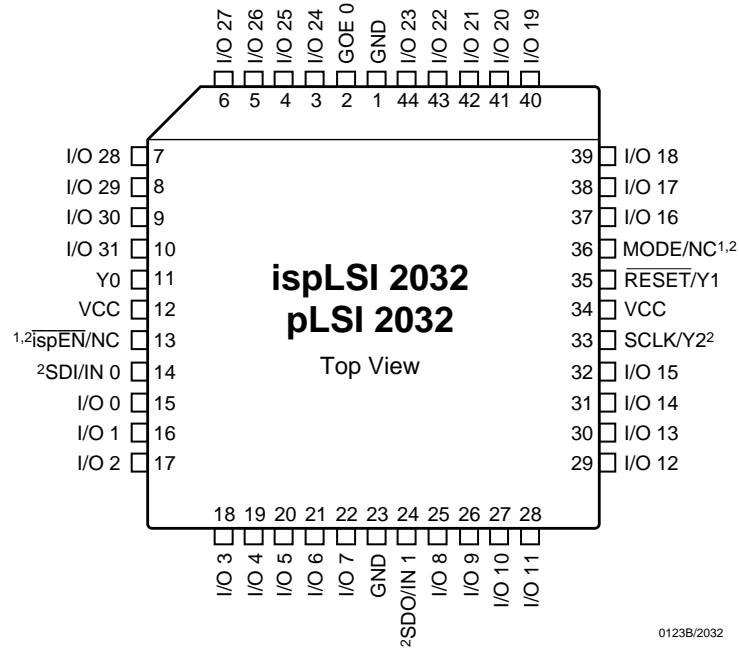
Pin Description

NAME	44-PIN PLCC PIN NUMBERS	44-PIN TQFP PIN NUMBERS	48-PIN TQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 23, 24, 25, 26, 31, 32, 33, 34, 35, 36, 37, 38, 41, 42, 43, 44, 1, 2, 3, 4	9, 10, 11, 13, 14, 15, 16, 17, 20, 21, 22, 23, 25, 26, 27, 28, 33, 34, 35, 37, 38, 39, 40, 41, 44, 45, 46, 47, 1, 2, 3, 4	Input/Output Pins — These are the general purpose I/O pins used by the logic array.
GOE 0	2	40	43	Global Output Enable input pin.
Y0	11	5	5	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device.
$\overline{RESET}$/Y1	35	29	31	This pin performs two functions: - Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O - Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
$\overline{ispEN}$/NC[1,2]	13	7	7	Input — Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK controls become active.
SDI/IN 0[2]	14	8	8	Input — This pin performs two functions. When $\overline{ispEN}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN0 also is used as one of the two control pins for the isp state machine. When $\overline{ispEN}$ is high, it functions as a dedicated input pin.
MODE/NC[2]	36	30	32	Input — When in ISP Mode, controls operation of ISP state machine.
SDO/IN 1[2]	24	18	19	Output/Input — This pin performs two functions. When $\overline{ispEN}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{ispEN}$ is high, it functions as a dedicated input pin.
SCLK/Y2[2]	33	27	29	Input — This pin performs two functions. When $\overline{ispEN}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{ispEN}$ is high, it functions as a dedicated clock input. This clock input is brought into the Clock Distribution Network and can be routed to any GLB and/or I/O cell on the device.
GND	1, 23	17, 39	18, 42	Ground (GND)
VCC	12, 34	6, 28	6, 30	V_{CC}
NC[1]			12, 24, 36, 48	No Connect.

Table 2-0002A-08isp/2032

1. NC pins are not to be connected to any active signals, VCC or GND.
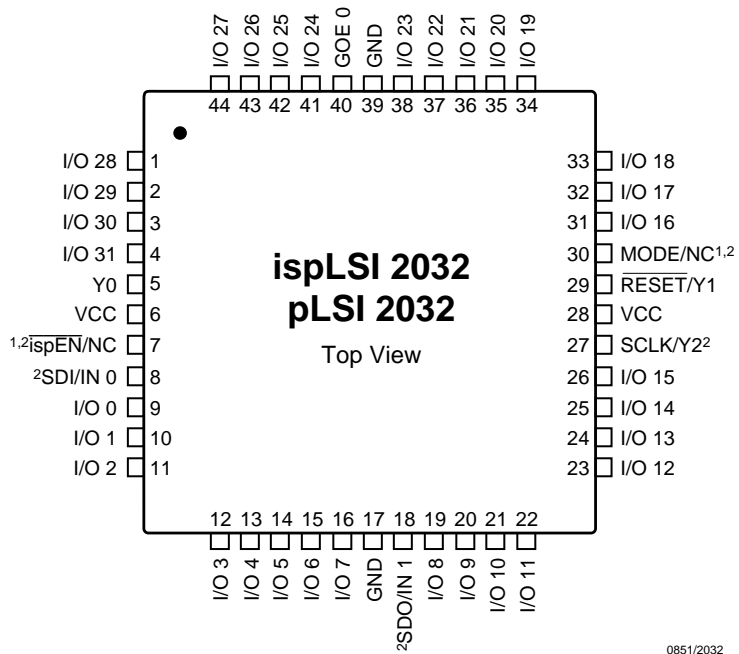2. Pins have dual function capability for ispLSI 2032 only.

Pin Configuration

ispLSI and pLSI 2032 44-Pin PLCC Pinout Diagram

Top row pins (6, 5, 4, 3, 2, 1, 44, 43, 42, 41, 40):
I/O 27, I/O 26, I/O 25, I/O 24, GOE 0, GND, I/O 23, I/O 22, I/O 21, I/O 20, I/O 19

Left side:
- I/O 28 — 7
- I/O 29 — 8
- I/O 30 — 9
- I/O 31 — 10
- Y0 — 11
- VCC — 12
- [1,2]$\overline{\text{ispEN}}$/NC — 13
- [2]SDI/IN 0 — 14
- I/O 0 — 15
- I/O 1 — 16
- I/O 2 — 17

Center: **ispLSI 2032 pLSI 2032** Top View

Right side:
- 39 — I/O 18
- 38 — I/O 17
- 37 — I/O 16
- 36 — MODE/NC[1,2]
- 35 — $\overline{\text{RESET}}$/Y1
- 34 — VCC
- 33 — SCLK/Y2[2]
- 32 — I/O 15
- 31 — I/O 14
- 30 — I/O 13
- 29 — I/O 12

Bottom row pins (18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28):
I/O 3, I/O 4, I/O 5, I/O 6, I/O 7, GND, [2]SDO/IN 1, I/O 8, I/O 9, I/O 10, I/O 11

0123B/2032

1. NC pins are not to be conneccted to any active signals, Vcc or GND.
2. Pins have dual function capability for ispLSI 2032 only (except pin 13, which is $\overline{\text{ispEN}}$ only).

ispLSI and pLSI 2032 44-Pin TQFP Pinout Diagram

Top row pins (44, 43, 42, 41, 40, 39, 38, 37, 36, 35, 34):
I/O 27, I/O 26, I/O 25, I/O 24, GOE 0, GND, I/O 23, I/O 22, I/O 21, I/O 20, I/O 19

Left side:
- I/O 28 — 1
- I/O 29 — 2
- I/O 30 — 3
- I/O 31 — 4
- Y0 — 5
- VCC — 6
- [1,2]$\overline{\text{ispEN}}$/NC — 7
- [2]SDI/IN 0 — 8
- I/O 0 — 9
- I/O 1 — 10
- I/O 2 — 11

Center: **ispLSI 2032 pLSI 2032** Top View

Right side:
- 33 — I/O 18
- 32 — I/O 17
- 31 — I/O 16
- 30 — MODE/NC[1,2]
- 29 — $\overline{\text{RESET}}$/Y1
- 28 — VCC
- 27 — SCLK/Y2[2]
- 26 — I/O 15
- 25 — I/O 14
- 24 — I/O 13
- 23 — I/O 12

Bottom row pins (12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22):
I/O 3, I/O 4, I/O 5, I/O 6, I/O 7, GND, [2]SDO/IN 1, I/O 8, I/O 9, I/O 10, I/O 11

0851/2032

1. NC pins are not to be connected to any active signal, Vcc or GND.
2. Pins have dual function capability for ispLSI 2032 only (except pin 7, which is $\overline{\text{ispEN}}$ only).

Pin Configuration

ispLSI 2032 48-Pin TQFP Pinout Diagram

Top-side pins (48–37): NC[1], I/O 27, I/O 26, I/O 25, I/O 24, GOE 0, GND, I/O 23, I/O 22, I/O 21, I/O 20, I/O 19

Left-side pins (1–12):
- 1 — I/O 28
- 2 — I/O 29
- 3 — I/O 30
- 4 — I/O 31
- 5 — Y0
- 6 — VCC
- 7 — $\overline{\text{ispEN}}$
- 8 — [2]SDI/IN 0
- 9 — I/O 0
- 10 — I/O 1
- 11 — I/O 2
- 12 — [1]NC

Right-side pins (36–25):
- 36 — NC[1]
- 35 — I/O 18
- 34 — I/O 17
- 33 — I/O 16
- 32 — MODE
- 31 — $\overline{\text{RESET}}$/Y1[2]
- 30 — VCC
- 29 — SCLK/Y2[2]
- 28 — I/O 15
- 27 — I/O 14
- 26 — I/O 13
- 25 — I/O 12

Bottom-side pins (13–24): I/O 3, I/O 4, I/O 5, I/O 6, I/O 7, GND, [2]SDO/IN 1, I/O 8, I/O 9, I/O 10, I/O 11, [1]NC

ispLSI 2032
Top View

48-Pin TQFP-2032

1. NC pins are not to be connected to any active signal, Vcc or GND.
2. Pins have dual function capability.

Part Number Description

(is)pLSI   2032 – XXX   X   XXX   X

Device Family

Device Number

Speed
180 = 180 MHz **f**max
150 = 154 MHz **f**max
135 = 137 MHz **f**max
110 = 111 MHz **f**max
 80 = 84 MHz **f**max

Grade
 Blank = Commercial
 I = Industrial

Package
 J = PLCC
 T = TQFP
 T44 = TQFP
 T48 = TQFP

Power
 L = Low
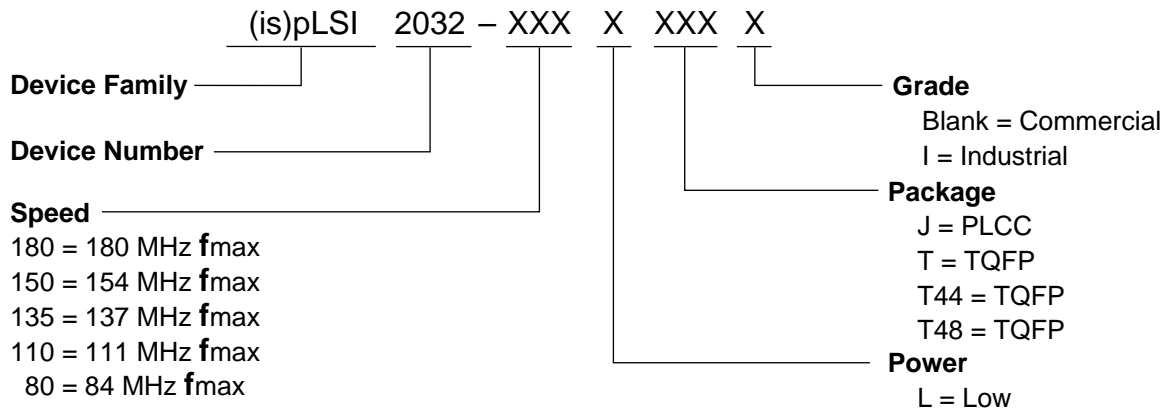
0212/2032

ispLSI and pLSI 2032 Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	180	5.0	ispLSI 2032-180LJ	44-Pin PLCC
	180	5.0	ispLSI 2032-180 LT44	44-Pin TQFP
	180	5.0	ispLSI 2032-180LT48	48-Pin TQFP
	154	5.5	ispLSI 2032-150LJ	44-Pin PLCC
	154	5.5	ispLSI 2032-150LT	44-Pin TQFP
	154	5.5	ispLSI 2032-150LT44	44-Pin TQFP
	154	5.5	ispLSI 2032-150LT48	48-Pin TQFP
	137	7.5	ispLSI 2032-135LJ	44-Pin PLCC
	137	7.5	ispLSI 2032-135LT	44-Pin TQFP
	137	7.5	ispLSI 2032-135LT44	44-Pin TQFP
	137	7.5	ispLSI 2032-135LT48	48-Pin TQFP
	111	10	ispLSI 2032-110LJ	44-Pin PLCC
	111	10	ispLSI 2032-110LT	44-Pin TQFP
	111	10	ispLSI 2032-110LT44	44-Pin TQFP
	111	10	ispLSI 2032-110LT48	48-Pin TQFP
	84	15	ispLSI 2032-80LJ	44-Pin PLCC
	84	15	ispLSI 2032-80LT	44-Pin TQFP
	84	15	ispLSI 2032-80LT44	44-Pin TQFP
	84	15	ispLSI 2032-80LT48	48-Pin TQFP
pLSI	180	5.0	pLSI 2032-180LJ	44-Pin PLCC
	154	5.5	pLSI 2032-150LJ	44-Pin PLCC
	154	5.5	pLSI 2032-150LT	44-Pin TQFP
	154	5.5	pLSI 2032-150LT44	44-Pin TQFP
	137	7.5	pLSI 2032-135LJ	44-Pin PLCC
	137	7.5	pLSI 2032-135LT	44-Pin TQFP
	137	7.5	pLSI 2032-135LT44	44-Pin TQFP
	111	10	pLSI 2032-110LJ	44-Pin PLCC
	111	10	pLSI 2032-110LT	44-Pin TQFP
	111	10	pLSI 2032-110LT44	44-Pin TQFP
	84	15	pLSI 2032-80LJ	44-Pin PLCC
	84	15	pLSI 2032-80LT	44-Pin TQFP
	84	15	pLSI 2032-80LT44	44-Pin TQFP

Table 2-0041A/2032

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	84	15	ispLSI 2032-80LJI	44-Pin PLCC
	84	15	ispLSI 2032-80LT44I	44-Pin TQFP
	84	15	ispLSI 2032-80LT48I	48-Pin TQFP

Table 2-0041B-08isp/2000