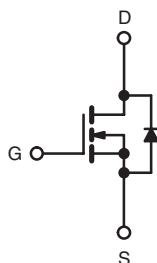
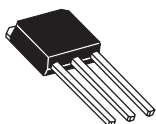




Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	3.0
Q_g (Max.) (nC)	19	
Q_{gs} (nC)	3.3	
Q_{gd} (nC)	13	
Configuration	Single	

DPAK
(TO-252)IPAK
(TO-251)

N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR420/SiHFR420)
- Straight Lead (IRFU420/SiHFU420)
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling
- Lead (Pb)-free Available

RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU/SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRFR420PbF	IRFR420TRPbF ^a	IRFR120TRLpBf ^a	IRFU420PbF
	SiHFR420-E3	SiHFR420T-E3 ^a	SiHFR120TL-E3 ^a	SiHFU420-E3
SnPb	IRFR420	IRFR420TR ^a	IRFR120TRL ^a	IRFU420
	SiHFR420	SiHFR420T ^a	SiHFR120TL ^a	SiHFU420

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	500	V
Gate-Source Voltage			V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	2.4	A
		T _C = 100 °C		1.5	
Pulsed Drain Current ^a			I _{DM}	8.0	
Linear Derating Factor				0.33	W/°C
Linear Derating Factor (PCB Mount) ^e				0.020	
Single Pulse Avalanche Energy ^b			E _{AS}	400	mJ
Repetitive Avalanche Current ^a			I _{AR}	2.4	A
Repetitive Avalanche Energy ^a			E _{AR}	4.2	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	42	W
Maximum Power Dissipation (PCB Mount) ^e	T _A = 25 °C			2.5	
Peak Diode Recovery dV/dt ^c			dV/dt	3.5	V/ns

* Pb containing terminations are not RoHS compliant, exemptions may apply

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	260 ^d	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 124\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 2.4\text{ A}$ (see fig. 12).
c. $I_{SD} \leq 2.4\text{ A}$, $di/dt \leq 50\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^{\circ}\text{C}$.
d. 1.6 mm from case.
e. When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	110	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	50	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.0	

Note

- a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$	-	0.59	-	$\text{V}/^{\circ}\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 1.4\text{ A}^b$	-	-	3.0	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 1.4\text{ A}$	1.5	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	360	-	pF
Output Capacitance	C_{oss}		-	92	-	
Reverse Transfer Capacitance	C_{rss}		-	37	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 2.1\text{ A}$, $V_{DS} = 400\text{ V}$, see fig. 6 and 13 ^b	-	-	19	nC
Gate-Source Charge	Q_{gs}		-	-	3.3	
Gate-Drain Charge	Q_{gd}		-	-	13	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$, $I_D = 2.1\text{ A}$, $R_G = 18\text{ }\Omega$, $R_D = 120\text{ }\Omega$, see fig. 10 ^b	-	8.0	-	ns
Rise Time	t_r		-	8.6	-	
Turn-Off Delay Time	$t_{d(off)}$		-	33	-	
Fall Time	t_f		-	16	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	





SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	2.4	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	8.0	
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}$, $I_S = 2.4\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$, $I_F = 2.1\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	260	520	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.70	1.4	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

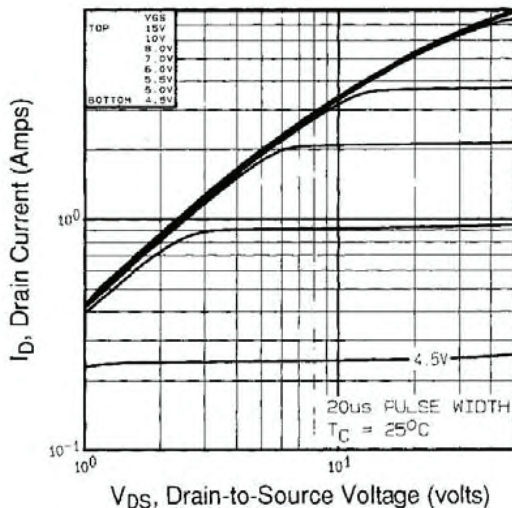


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

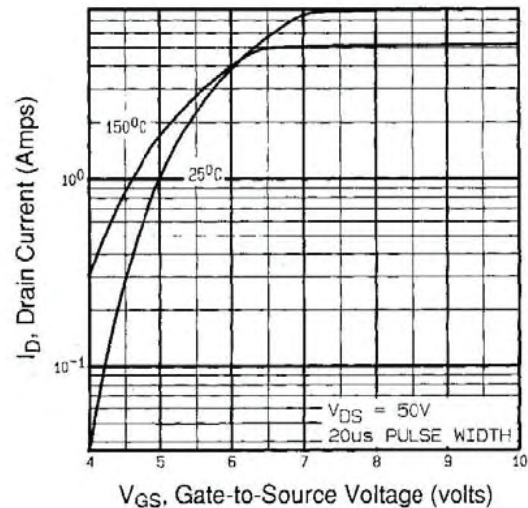


Fig. 3 - Typical Transfer Characteristics

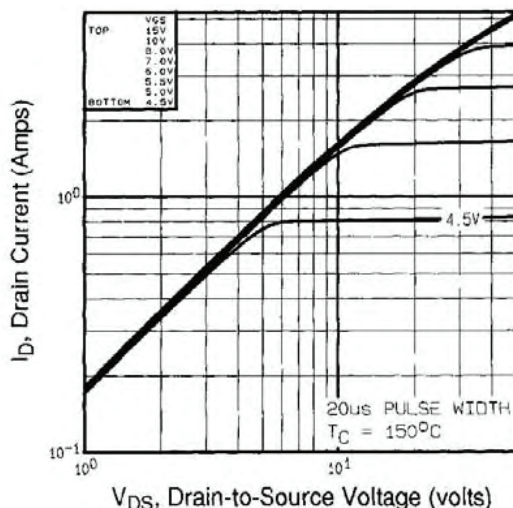


Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

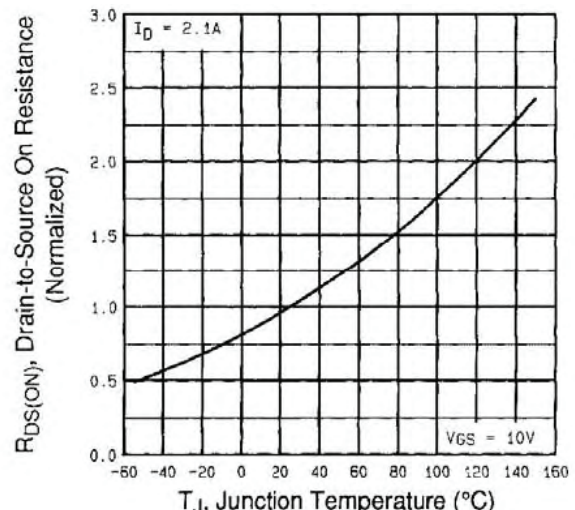


Fig. 4 - Normalized On-Resistance vs. Temperature

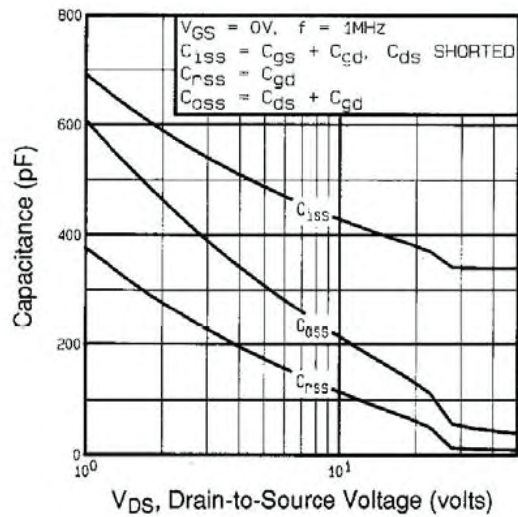


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

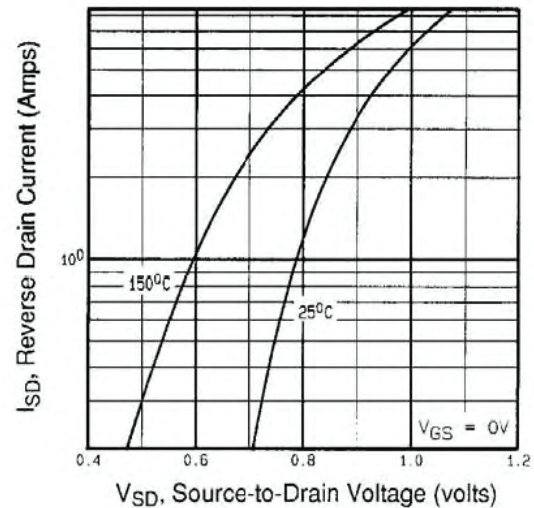


Fig. 7 - Typical Source-Drain Diode Forward Voltage

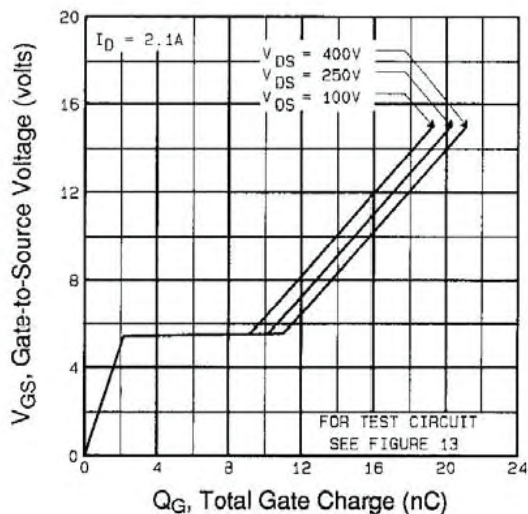


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

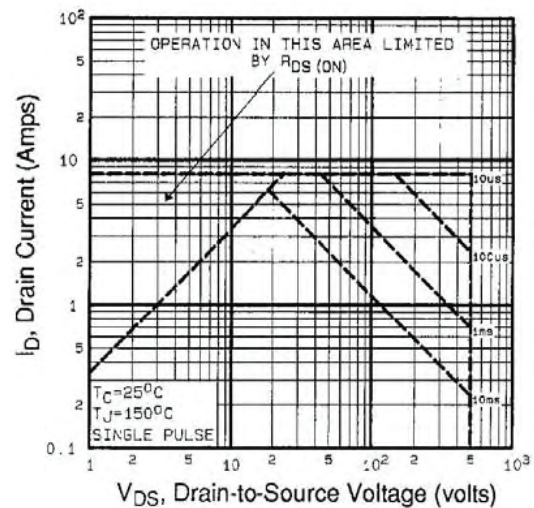


Fig. 8 - Maximum Safe Operating Area

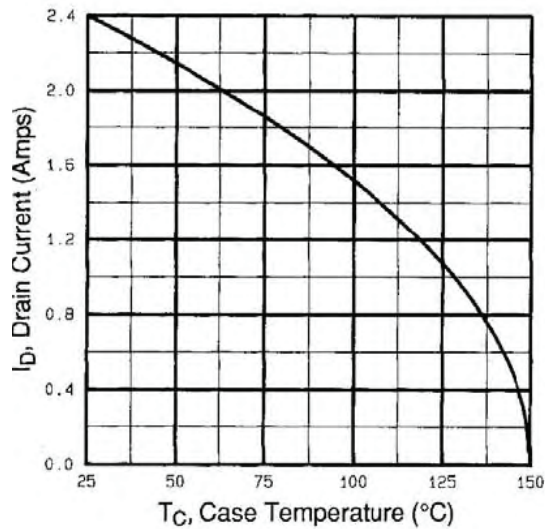


Fig. 9 - Maximum Drain Current vs. Case Temperature

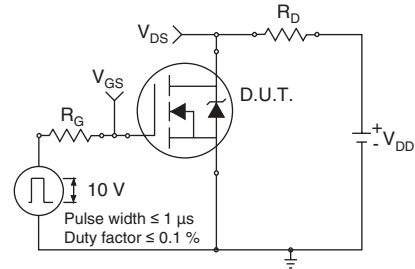


Fig. 10a - Switching Time Test Circuit

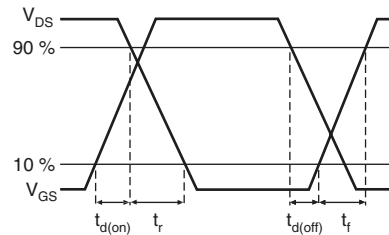


Fig. 10b - Switching Time Waveforms

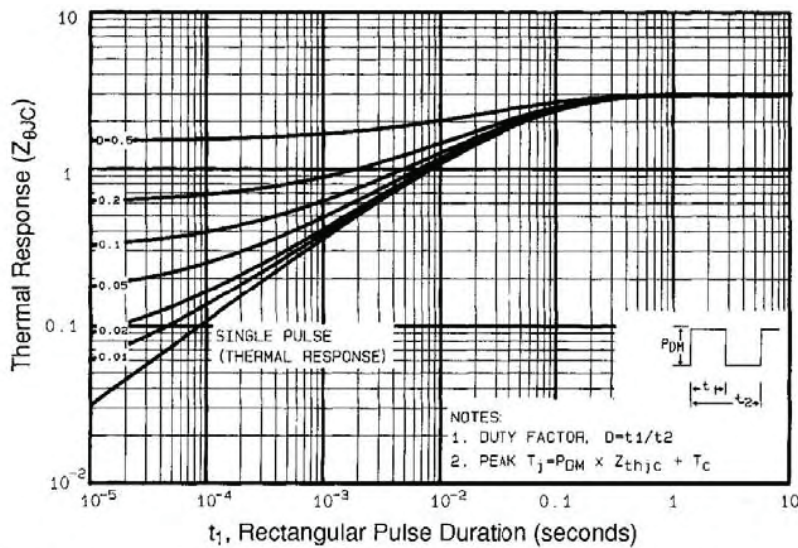


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

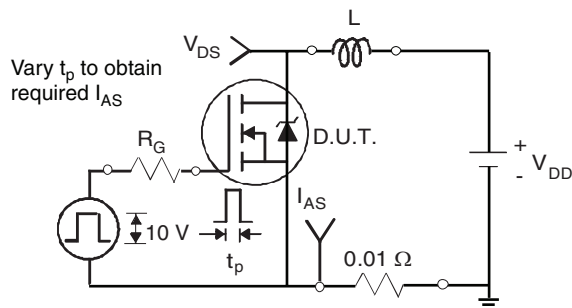


Fig. 12a - Unclamped Inductive Test Circuit

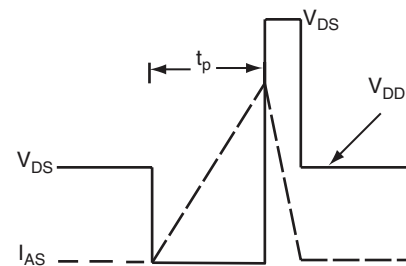


Fig. 12b - Unclamped Inductive Waveforms

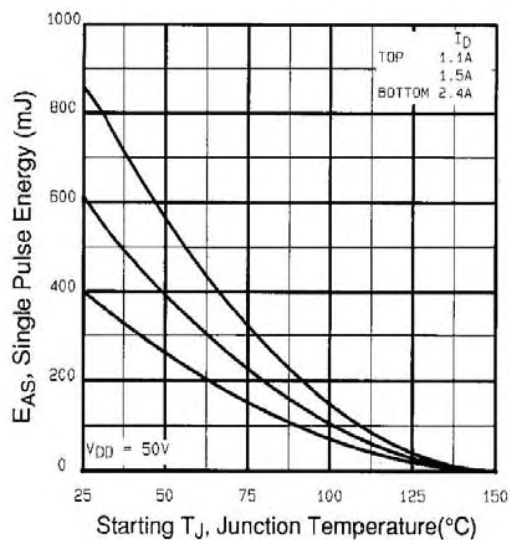


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

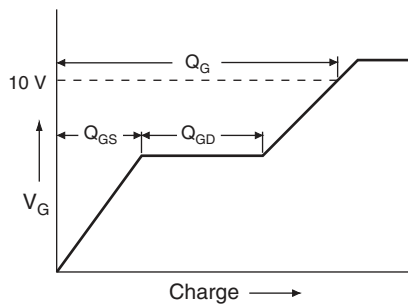


Fig. 13a - Basic Gate Charge Waveform

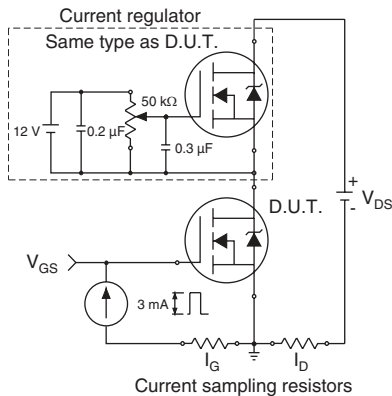
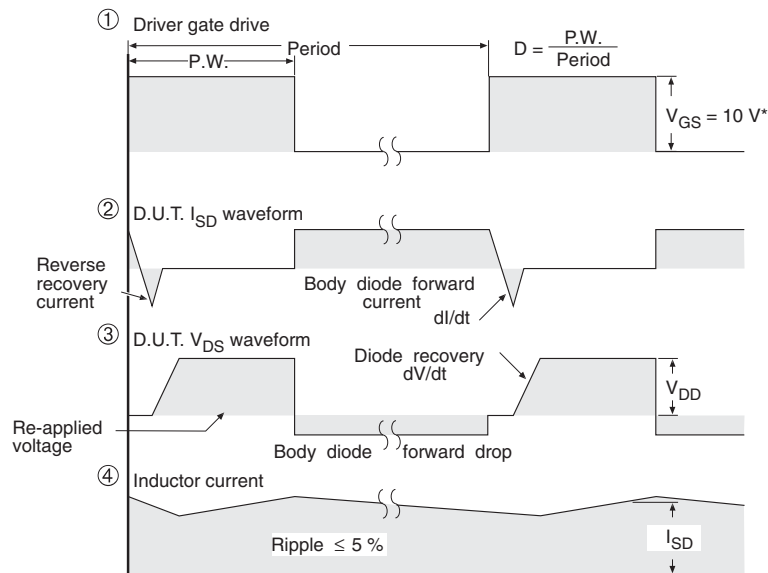
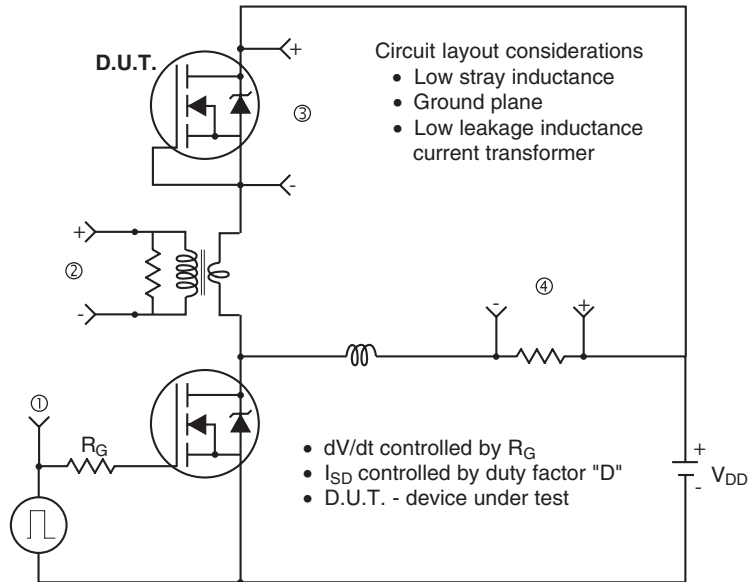


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices and $3 V$ drive devices

Fig. 14 -For N-Channel

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