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# **Am27C128** 128 Kilobit (16 K x 8-Bit) CMOS EPROM

## DISTINCTIVE CHARACTERISTICS

#### Fast access time

- Speed options as fast as 45 ns

- Low power consumption
  - 20 µA typical CMOS standby current
- JEDEC-approved pinout
- Single +5 V power supply
- ±10% power supply tolerance standard
- 100% Flashrite<sup>™</sup> programming
  - Typical programming time of 2 seconds

- Latch-up protected to 100 mA from –1 V to V<sub>CC</sub> + 1 V
- High noise immunity
- Versatile features for simple interfacing
  - Both CMOS and TTL input/output compatibility
  - Two line control functions
- Standard 28-pin DIP, PDIP, and 32-pin PLCC packages

#### **GENERAL DESCRIPTION**

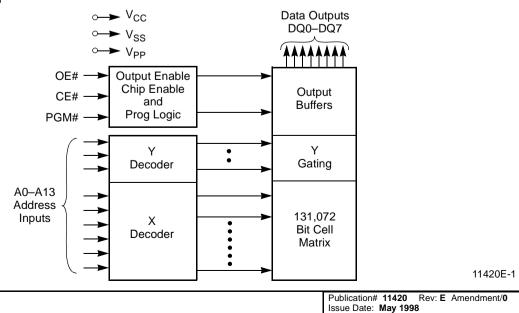
The Am27C128 is a 128-Kbit, ultraviolet erasable programmable read-only memory. It is organized as 16 Kwords by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP packages, as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Data can be typically accessed in less than 45 ns, allowing high-performance microprocessors to operate without any WAIT states. The device offers separate Output Enable (OE#) and Chip Enable (CE#) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100  $\mu$ W in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The device supports AMD's Flashrite programming algorithm (100  $\mu$ s pulses), resulting in a typical programming time of 2 seconds.

#### **BLOCK DIAGRAM**



This datasheet has been downloaded from http://www.digchip.com at this page

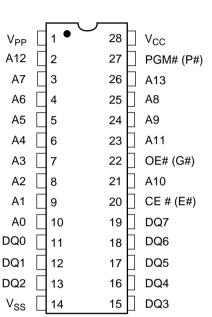
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# PRODUCT SELECTOR GUIDE

Family Part Num				Am27C128						
Speed Options	$V_{CC} = 5.0 \text{ V} \pm 5\%$								-255	
	$V_{CC}=5.0~V\pm10\%$	-45	-55	-70	-90	-120	-150	-200		
Max Access Time (ns)		45	55	70	90	120	150	200	250	
CE# (E#) Access (ns)		45	55	70	90	120	150	200	250	
OE# (G#) Access (ns)		30	35	40	40	50	50	50	50	

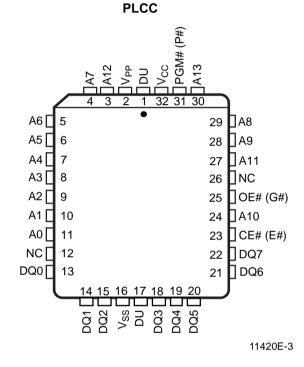
### **CONNECTION DIAGRAMS**

# **Top View**



DIP

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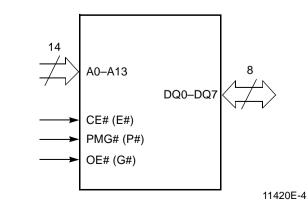
#### Notes:

- 1. JEDEC nomenclature is in parenthesis.
- 2. Don't use (DU) for PLCC.

#### **PIN DESIGNATIONS**

A0–A13	= Address Inputs
CE# (E#)	= Chip Enable Input
DQ0–DQ7	= Data Input/Outputs
OE# (G#)	<ul> <li>Output Enable Input</li> </ul>
PGM# (P#)	= Program Enable Input
V <sub>CC</sub>	= V <sub>CC</sub> Supply Voltage
V <sub>PP</sub>	= Program Voltage Input
V <sub>SS</sub>	= Ground
NC	= No Internal Connection

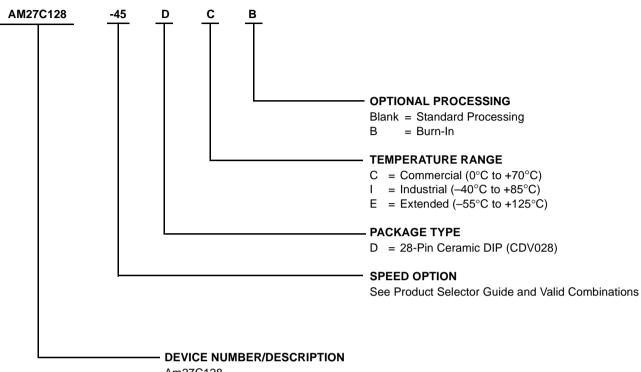
#### LOGIC SYMBOL



# **ORDERING INFORMATION**

# **UV EPROM Products**

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Am27C128 128 Kilobit (16 K x 8-Bit) CMOS UV EPROM

Valid C	ombinations				
AM27C128-45	DC, DCB, DI, DIB				
AM27C128-55	DC, DCD, DI, DIB				
AM27C128-70					
AM27C128-90					
AM27C128-120	DC, DCB, DI, DIB, DE, DEB				
AM27C128-150					
AM27C128-200					
AM27C128-255 V <sub>CC</sub> = 5.0 V ± 5%	DC, DCB, DI, DIB				

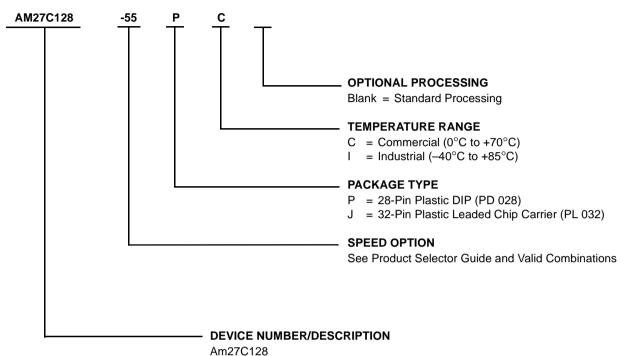
#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

#### **ORDERING INFORMATION**

### **OTP EPROM Products**

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



128 Kilobit (16 K x 8-Bit) CMOS OTP EPROM

Valid Combinations						
AM27C128-55						
AM27C128-70						
AM27C128-90						
AM27C128-120	JC, PC, JI, PI					
AM27C128-150	, , , ,					
AM27C128-200						
AM27C128-255 V <sub>CC</sub> = 5.0 V ± 5%						

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

#### FUNCTIONAL DESCRIPTION

#### **Device Erasure**

In order to clear all locations of their programmed contents, the device must be exposed to an ultraviolet light source. A dosage of 15 W seconds/cm<sup>2</sup> is required to completely erase the device. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000  $\mu$ W/cm<sup>2</sup> for 15 to 20 minutes. The device should be directly under and about one inch from the source, and all filters should be removed from the UV light source prior to erasure.

Note that all UV erasable devices will erase with light sources having wavelengths shorter than 4000 Å, such as fluorescent light and sunlight. Although the erasure process happens over a much longer time period, exposure to any light source should be prevented for maximum system reliability. Simply cover the package window with an opaque label or substance.

#### **Device Programming**

Upon delivery, or after each erasure, the device has all of its bits in the "ONE", or HIGH state. "ZEROs" are loaded into the device through the programming procedure.

The device enters the programming mode when 12.75 V  $\pm$  0.25 V is applied to the V\_PP pin, and CE# and PGM# are at V\_IL.

For programming, the data to be programmed is applied 8 bits in parallel to the data pins.

The flowchart in the Programming section of the EPROM Products Data Book (Section 5, Figure 5-1) shows AMD's Flashrite algorithm. The Flashrite algorithm reduces programming time by using a 100 µs programming pulse and by giving each address only as many pulses to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum pulses allowed is reached. This process is repeated while sequencing through each address of the device. This part of the algorithm is done at  $V_{CC}$  = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at  $V_{CC} = V_{PP} =$ 5.25 V.

Please refer to Section 5 of the EPROM Products Data Book for additional programming information and specifications.

#### **Program Inhibit**

Programming different data to multiple devices in parallel is easily accomplished. Except for CE#, all like inputs of the devices may be common. A TTL low-level program pulse applied to one device's CE# input with  $V_{PP}$  = 12.75 V ± 0.25 V and PGM# LOW will program that particular device. A high-level CE# input inhibits the other devices from being programmed.

#### **Program Verify**

A verification should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with OE# and CE#, at V<sub>IL</sub>, PGM# at V<sub>IH</sub>, and V<sub>PP</sub> between 12.5 V and 13.0 V.

#### Autoselect Mode

The autoselect mode provides manufacturer and device identification through identifier codes on DQ0–DQ7. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C  $\pm$  5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force V<sub>H</sub> on address line A9. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V<sub>IL</sub> to V<sub>IH</sub> (that is, changing the address from 00h to 01h). All other address lines must be held at V<sub>IL</sub> during the autoselect mode.

Byte 0 (A0 =  $V_{IL}$ ) represents the manufacturer code, and Byte 1 (A0 =  $V_{IH}$ ), the device identifier code. Both codes have odd parity, with DQ7 as the parity bit.

#### **Read Mode**

To obtain data at the device outputs, Chip Enable (CE#) and Output Enable (OE#) must be driven low. CE# controls the power to the device and is typically used to select the device. OE# enables the device to output data, independent of device selection. Addresses must be stable for at least  $t_{ACC}$ - $t_{OE}$ . Refer to the Switching Waveforms section for the timing diagram.

#### **Standby Mode**

The device enters the CMOS standby mode when CE# is at V<sub>CC</sub>  $\pm$  0.3 V. Maximum V<sub>CC</sub> current is reduced to 100 µA. The device enters the TTL-standby mode when CE# is at V<sub>IH</sub>. Maximum V<sub>CC</sub> current is reduced to 1.0 mA. When in either standby mode, the device places its outputs in a high-impedance state, independent of the OE# input.

#### **Output OR-Tieing**

To accommodate multiple memory connections, a two-line control function provides:

- Low memory power dissipation, and
- Assurance that output bus contention will not occur.

CE# should be decoded and used as the primary device-selecting function, while OE# be made a common

# 

connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

#### **System Applications**

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of

# MODE SELECT TABLE

these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1  $\mu F$  ceramic capacitor (high frequency, low inherent inductance) should be used on each device between  $V_{CC}$  and  $V_{SS}$  to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7  $\mu F$  bulk electrolytic capacitor should be used between  $V_{CC}$  and  $V_{SS}$  for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode		CE#	OE#	PGM#	A0	A9	V <sub>PP</sub>	Outputs	
Read		V <sub>IL</sub>	V <sub>IL</sub>	х	Х	х	x	D <sub>OUT</sub>	
Output Disable		Х	V <sub>IH</sub>	х	Х	х	х	High Z	
Standby (TTL)		V <sub>IH</sub>	Х	Х	х	Х	х	High Z	
Standby (CMOS)		$V_{CC} \pm 0.3 V$	Х	х	х	х	х	High Z	
Program		V <sub>IL</sub>	Х	V <sub>IL</sub>	х	х	V <sub>PP</sub>	D <sub>IN</sub>	
Program Ve	rify	VIL	V <sub>IL</sub>	V <sub>IH</sub>	х	х	V <sub>PP</sub>	D <sub>OUT</sub>	
Program Inhibit		V <sub>IH</sub>	Х	Х	х	Х	V <sub>PP</sub>	High Z	
Autoselect (Note 3)	Manufacturer Code	VIL	V <sub>IL</sub>	Х	V <sub>IL</sub>	V <sub>H</sub>	х	01h	
	Device Code	V <sub>IL</sub>	V <sub>IL</sub>	Х	V <sub>IH</sub>	V <sub>H</sub>	Х	16h	

#### Notes:

1.  $V_H = 12.0 V \pm 0.5 V.$ 

2.  $X = Either V_{IH} or V_{IL}$ .

3. A1–A8 and A10–12 = V<sub>IL</sub>, A13 = X

4. See DC Programming Characteristics for V<sub>PP</sub> voltage during programming.

#### **ABSOLUTE MAXIMUM RATINGS**

Storage Temperature
OTP Products65°C to +125°C
All Other Products65°C to +150°C
Ambient Temperature
with Power Applied $\dots -55^{\circ}C$ to $+125^{\circ}C$
Voltage with Respect to V <sub>SS</sub>
All pins except A9, V_PP, V_CC $\ldots$ -0.6 V to V_CC + 0.6 V
A9 and V_PP (Note 2) $\ldots \ldots \ldots -0.6$ V to 13.5 V
$V_{CC}$ (Note 1)
Notes:

- 1. Minimum DC voltage on input or I/O pins –0.5 V. During voltage transitions, the input may overshoot  $V_{SS}$  to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is  $V_{CC}$  + 5 V. During voltage transitions, input and I/O pins may overshoot to  $V_{CC}$  + 2.0 V for periods up to 20 ns.
- Minimum DC input voltage on A9 is –0.5 V. During voltage transitions, A9 and V<sub>PP</sub> may overshoot V<sub>SS</sub> to –2.0 V for periods of up to 20 ns. A9 and V<sub>PP</sub> must not exceed +13.5 V at any time.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum ratings for extended periods may affect device reliability.

#### **OPERATING RANGES**

Commercial (C) Devices
Ambient Temperature (T <sub>A</sub> ) $\dots \dots \dots 0^{\circ}$ C to +70°C
Industrial (I) Devices
Ambient Temperature (T <sub>A</sub> )40°C to +85°C
Extended (E) Devices
Ambient Temperature (T <sub>A</sub> ) $\dots -55^{\circ}C$ to +125°C
Supply Read Voltages
$V_{CC}$ for ± 5% devices +4.75 V to +5.25 V
$V_{CC}$ for ± 10% devices +4.50 V to +5.50 V
Operating ranges define these limits between which the func-

Operating ranges define those limits between which the functionality of the device is guaranteed.

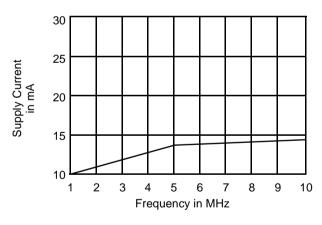
#### DC CHARACTERISTICS over operating range (unless otherwise specified)

Parameter Symbol	Parameter Description	Test Condition	Min	Мах	Unit	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -400 μA				V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA		0.45	V	
V <sub>IH</sub>	Input HIGH Voltage				V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage				+0.8	V
ILI	Input Load Current	$V_{IN} = 0 V \text{ to } V_{CC}$			1.0	μA
1			C/I Devices		1.0	
ILO	Output Leakage Current	$V_{OUT} = 0 V \text{ to } V_{CC}$	E Devices		5.0	μA
I <sub>CC1</sub>	V <sub>CC</sub> Active Current (Note 2)	CE# = V <sub>IL</sub> , f = 10 MHz, I <sub>OUT</sub> = 0 mA			25	mA
I <sub>CC2</sub>	V <sub>CC</sub> TTL Standby Current	CE# = V <sub>IH</sub>		1.0	mA	
I <sub>CC3</sub>	V <sub>CC</sub> CMOS Standby Current	$CE\#=V_{CC}\pm0.3\;V$		100	μA	
I <sub>PP1</sub>	V <sub>PP</sub> Supply Current (Read)	$CE\# = OE\# = V_{IL}, V_{PP} = V_{CC}$			100	μA

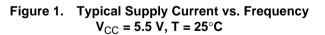
**Caution**: The device must not be removed from (or inserted into) a socket when  $V_{CC}$  or  $V_{PP}$  is applied.

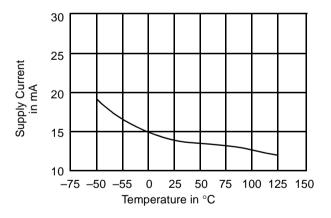
#### Notes:

- 1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
- 2.  $I_{CC1}$  is tested with  $OE = V_{IH}$  to simulate open outputs.
- Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V<sub>CC</sub> + 0.5 V, which may overshoot to V<sub>CC</sub> + 2.0 V for periods less than 20 ns.

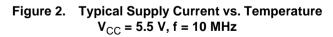




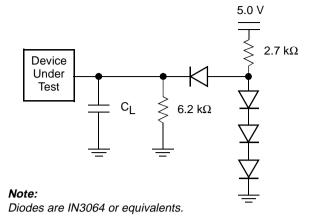




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#### **TEST CONDITIONS**



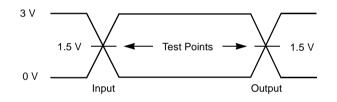
11420E-7

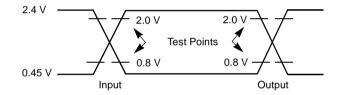
Figure 3. Test Setup

Table 1.	Test	Specifications
	ICOL	opecifications

Test Condition	-45, -55, -70	All others	Unit		
Output Load	1 TTL gate				
Output Load Capacitance, C <sub>L</sub> (including jig capacitance)	30	100	pF		
Input Rise and Fall Times	$\leq 2$	20	ns		
Input Pulse Levels	0.0–3.0	0.0–3.0 0.45–2.4			
Input timing measurement reference levels	1.5	0.8, 2.0	V		
Output timing measurement reference levels	1.5	0.8, 2.0	V		

#### SWITCHING TEST WAVEFORM





**Note:** For  $C_L = 30 \text{ pF}$ .

**Note:** For  $C_L = 100 \text{ pF}$ .

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### **KEY TO SWITCHING WAVEFORMS**

WAVEFORM	INPUTS	OUTPUTS			
	Steady				
	Cha	anging from H to L			
	Changing from L to H				
XXXXXX	Don't Care, Any Change Permitted Changing, State Unknown				
$\longrightarrow \longleftarrow$	Does Not Apply	Center Line is High Impedance State (High Z)			

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# **AC CHARACTERISTICS**

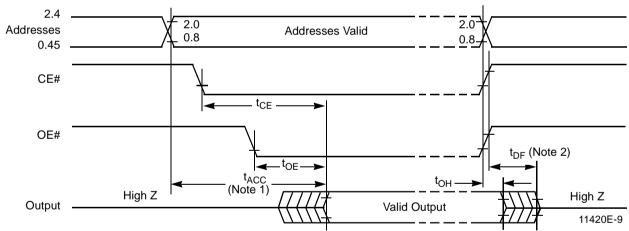
Paramete	er Symbols							Am27	7C128				
JEDEC	Standard	Description	Test Setup		-45	-55	-70	-90	-120	-150	-200	-255	Unit
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address to Output Delay	CE#, OE# = V <sub>IL</sub>	Max	45	55	70	90	120	150	200	250	ns
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable to Output Delay	OE# = V <sub>IL</sub>	Max	45	55	70	90	120	150	200	250	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Output Delay	CE# = V <sub>IL</sub>	Max	30	35	40	40	50	50	50	50	ns
t <sub>EHQZ</sub> t <sub>GHQZ</sub>	t <sub>DF</sub> (Note 2)	Chip Enable High or Output Enable High to Output High Z, Whichever Occurs First		Max	25	25	25	25	30	30	30	30	ns
t <sub>AXQX</sub>	t <sub>OH</sub>	Output Hold Time from Addresses, CE# or OE#, Whichever Occurs First		Min	0	0	0	0	0	0	0	0	ns

*Caution:* Do not remove the device from (or insert it into) a socket or board that has  $V_{PP}$  or  $V_{CC}$  applied. *Notes:* 

1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ 

- 2. This parameter is sampled and not 100% tested.
- 3. Switching characteristics are over operating range, unless otherwise specified.
- 4. See Figure 3 and Table 1 for test specifications.

#### SWITCHING WAVEFORMS



#### Notes:

- 1. OE# may be delayed up to  $t_{ACC} t_{OE}$  after the falling edge of the addresses without impact on  $t_{ACC}$ .
- 2. t<sub>DF</sub> is specified from OE# or CE#, whichever occurs first.

#### PACKAGE CAPACITANCE

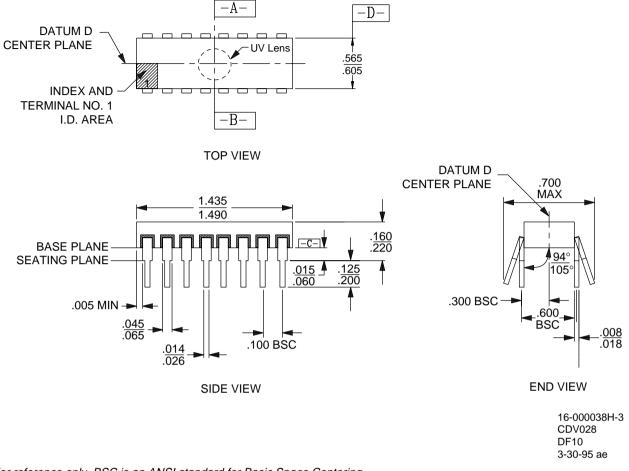
Parameter Symbol	Parameter Description	Test Conditions	CDV028		PL 032		PD 028		
			Тур	Max	Тур	Max	Тур	Max	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0	8	10	6	10	5	10	pF
C <sub>OUT</sub>	Output Capacitance	$V_{OUT} = 0$	11	14	8	12	8	10	pF

#### Notes:

- 1. This parameter is only sampled and not 100% tested.
- 2.  $T_A = +25^{\circ}C, f = 1 MHz.$

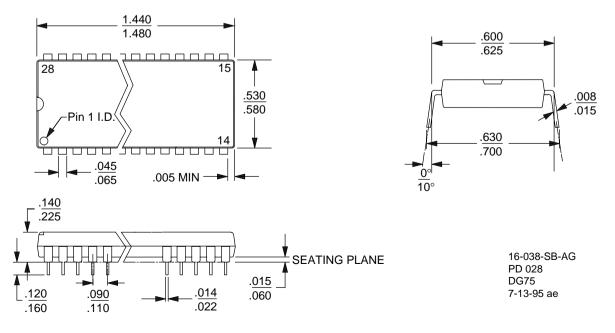
#### **PHYSICAL DIMENSIONS\***

#### CDV028—28-Pin Ceramic Dual In-Line Package, UV Lens (measured in inches)



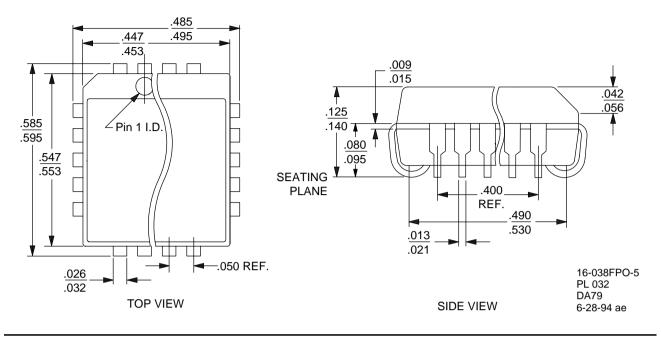
\* For reference only. BSC is an ANSI standard for Basic Space Centering.

### PD 028—28-Pin Plastic Dual In-Line Package (measured in inches)



# PHYSICAL DIMENSIONS

PL 032—32-Pin Plastic Leaded Chip Carrier (measured in inches)



#### **REVISION SUMMARY FOR AM27C128**

#### **Revision E**

#### Global

Changed formatting to match current data sheets.

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