8155(H)/8156(H)

2048-Bit Static MOS RAM with I/O Ports and Timer

DISTINCTIVE CHARACTERISTICS

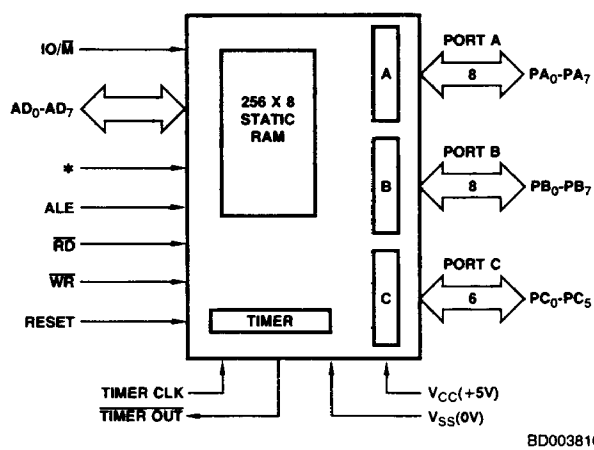
- 256 word x 8-bits
- Single +5 V power supply
- Completely static operation
- Internal address latch
- 2 programmable 8-bit I/O ports
- 1 programmable 6-bit I/O port
- Programmable 14-bit binary counter/timer
- Multiplexed address and data bus

GENERAL DESCRIPTION

The 8155(H) and 8156(H) are RAM and I/O chips to be used in the 8085AH MPU system. The RAM portion is designed with 2K bit static cells organized as 256 x 8. They have a maximum access time of 400ns to permit use with no wait states in 8085AH CPU. The 8155H-2 and 8156H-2 have maximum access times of 330ns for use with the 8085AH. The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

BLOCK DIAGRAM



*8155H = $\overline{CE}$, 8156H = CE

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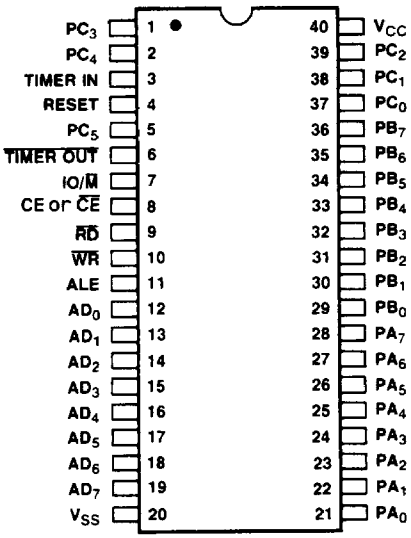
Issue Date: April 1987

CONNECTION DIAGRAM
Top View

DIPs



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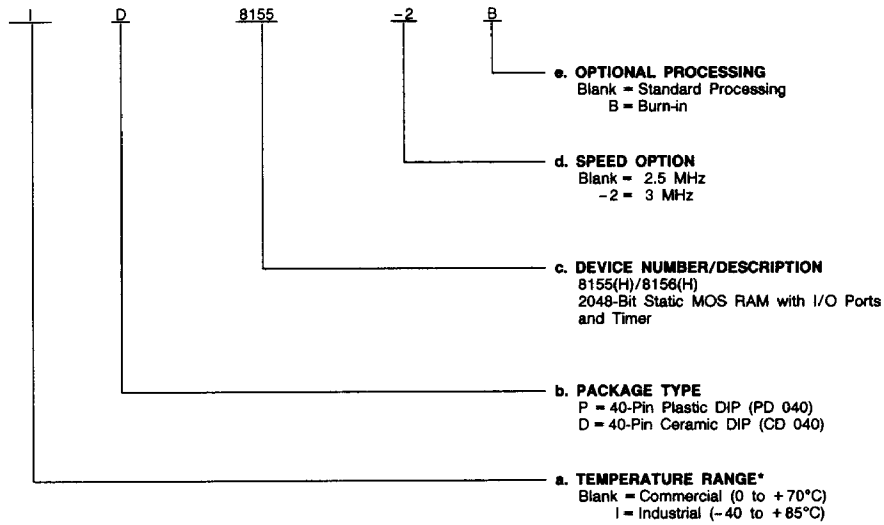
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Temperature Range**
b. Package Type
c. Device Number
d. Speed Option
e. Optional Processing



Valid Combinations	
P, D	8155
	8155H
	8155-2
	8155H-2
	8156
	8156H
	8156-2
	8156H-2
D, ID	8155B
	8155HB
	8155-2B
	8155H-2B
	8156B
	8156HB
	8156-2B
	8156H-2B

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

*This device is also available in Military temperature range. See MOS Microprocessors and Peripherals Military Handbook (Order #09275A/0) for electrical performance characteristics.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
4	RESET	I	The Reset signal is a pulse provided by the 8085AH to initialize the system. Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be 600ns. (Two 8085AH clock cycle times).
12-19	AD_0-AD_7	I/O	These are 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch on the falling edge of the ALE. The address can be either for the memory section or the I/O section depending on the polarity of the IO/$\overline{M}$ input signal. The 8-bit data is either written into the chip or read from the chip depending on the status of $\overline{WRITE}$ or $\overline{READ}$ input signal.
8	CE OR $\overline{CE}$	I	Chip Enable: On the 8155(H) this pin is $\overline{CE}$ and is active low. On the 8156(H) this pin is CE and is active high.
9	$\overline{RD}$	I	Input low on this line with the Chip Enable active enables the AD_{0-7} buffers. If IO/$\overline{M}$ pin is LOW, the RAM content will be read out to the AD bus. Otherwise, the content of the selected I/O port will be read to the AD bus.
10	$\overline{WR}$	I	Input low on this line with the Chip Enable active causes the data on the AD lines to be written to the RAM or I/O ports, depending on the polarity of IO/$\overline{M}$.
11	ALE	I	Address Latch Enable: This control signal latches the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
7	IO/$\overline{M}$	I	IO/$\overline{MEMORY}$ Select: This line selects the memory if LOW and selects the IO if HIGH.
21-28	PA_0-PA_7	I/O	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status Register.
29-36	PB_0-PB_7	I/O	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status Register.
37-39, 1, 2, 5	PC_0-PC_5	I/O	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the C/S Register. When PC_{0-5} are used as control signals, they will provide the following: PC_0-A INTR (Port A Interrupt) PC_1-A BF (Port A Buffer Full) PC_2-$\overline{A\ STB}$ (Port A Strobe) PC_3-B INTR (Port B Interrupt) PC_4-B BF (Port B Buffer Full) PC_5-$\overline{B\ STB}$ (Port B Strobe)
3	TIMER IN	I	This is the timer input to the counter timer.
6	$\overline{TIMER\ OUT}$	O	This pin is the timer output. This output can be either a square wave or a pulse depending on the timer mode.
40	V_{CC}		+5 volt supply.
20	V_{SS}		Ground reference.

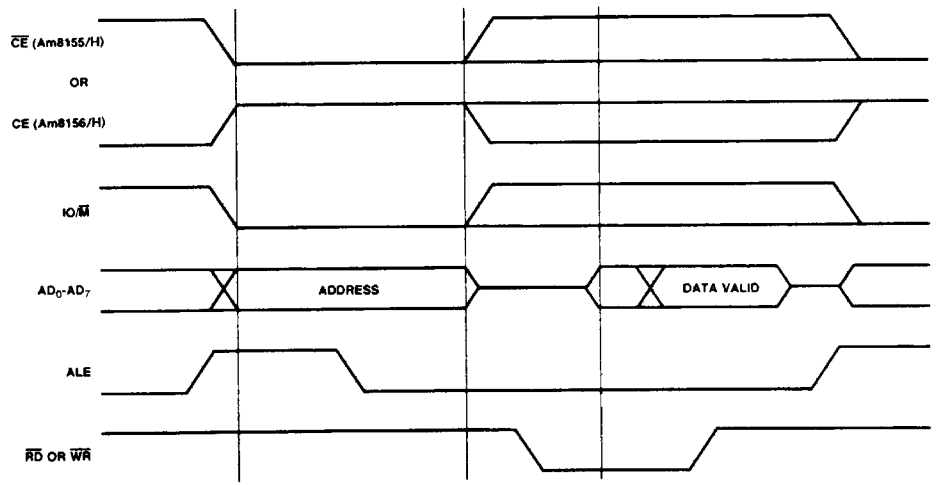
DETAILED DESCRIPTION

The 8155(H)/8156(H) includes the following operational features:

- 2K Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA and PB) and one 6-bit I/O port (PC)
- 14-bit down counter

The I/O portion contains four registers (Command/Status, PA_{0-7}, PB_{0-7}, PC_{0-5}). The IO/$\overline{M}$ (IO/$\overline{Memory}$ Select) pin selects the I/O or the memory (RAM) portion. Detailed descriptions of memory, I/O ports and timer functions will follow.

The 8-bit address on the AD lines, the Chip Enable input, and IO/$\overline{M}$ are all latched on chip at the falling edge of ALE. A LOW on the IO/$\overline{M}$ must be provided to select the memory section.



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Note: For detailed timing diagram information, see Read/Write Cycle Timing Diagrams and Switching Characteristics.

Figure 1. Memory Read/Write Cycle

PROGRAMMING INFORMATION

The Command/Status Register

The command register consists of eight latches, one for each bit. Four bits (0-3) define the mode of the ports. Two bits (4-5) enable or disable the interrupt from Port C when it acts as control port, and the last two bits (6-7) are for the timer.

The C/S register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation. The meaning of each bit of the command byte is defined as follows:

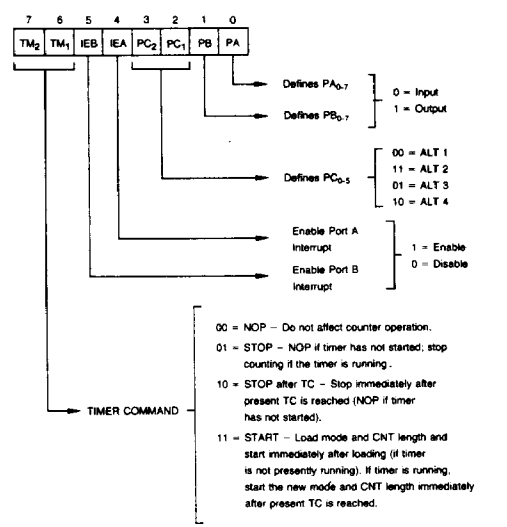

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Figure 2. Command/Status Register Bit Assignment

Reading the Command/Status Register

The status register consists of seven latches, one for each bit: six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the C/S Register (Address XXXXX000). Status word format is shown below:

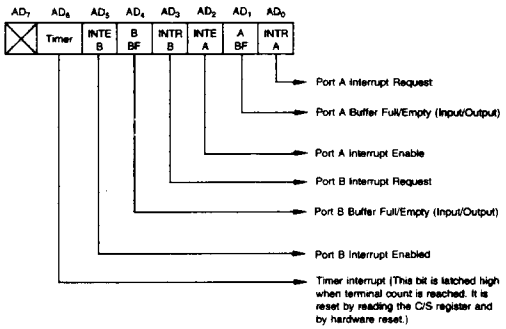

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Figure 3. Command/Status Register Status Word Format

Input/Output Section

The I/O section of the 8155(H)/8156(H) consists of four registers as described below.

- Command/Status Register (C/S) — This register is assigned the address XXXXXOOO. The C/S address serves a dual purpose.
  When the C/S register is selected during WRITE operation, a command is written into the command register. The contents of this register are not accessible through the pins.
  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD_{0-7} lines.
- PA Register — This register can be programmed to be either input or output ports, depending on the status of the contents of the C/S Register. Also, depending on the command, this port can operate in either the basic mode or the strobed mode (see timing diagram). The I/O pins assigned in relation to this register are PA_{0-7}. The address of this register is XXXXX001.
- PB Register — This register functions the same as PA Register. The I/O pins assigned are PB_{0-7}. The address of this register is XXXXX010.
- PC Register — This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB properly programming the AD_2 and AD_3 bits of the C/S register.
  When PC_{0-5} is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the 8155(H) sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. See Table 1.

When the "C" port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

Control	Input Mode	Output Mode
BF	LOW	LOW
INTR	LOW	HIGH
$\overline{STB}$	Input Control	Input Control

The set and reset of INTR and BF with respect to $\overline{STB}$, $\overline{WR}$ and $\overline{RD}$ timing are shown in Strobed I/O Timing Diagrams.

To summarize, the register's assignments are:

Address	Pinouts	Functions	No. of Bits
XXXXX000	Internal	Command/Status Register	8
XXXXX001	PA_{0-7}	General Purpose I/O Port	8
XXXXX010	PB_{0-7}	General Purpose I/O Port	8
XXXXX011	PC_{0-5}	General Purpose I/O Port or Control Lines	6

The following diagram shows how I/O Ports A and B are structured within the 8155(H) and 8156(H):

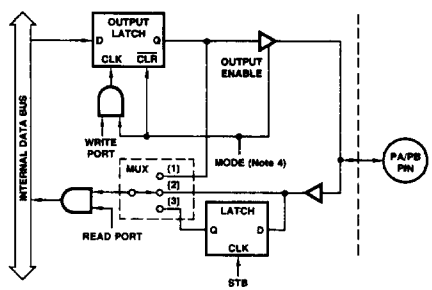

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Figure 4. 8155(H)/8156(H) One Bit of Port A or Port B

Notes: 1. Output Mode
2. Simple Input
3. Strobed Input

} Multiplexer Control

4. = 1 for output mode.
= 0 for input mode.

Read Port = (IO/$\overline{M}$ = 1) • ($\overline{RD}$ = 0) • (CE active) • (Port address selected)

Write Port = (IO/$\overline{M}$ = 1) • ($\overline{WR}$ = 0) • (CE active) • (Port address selected)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go LOW. When the 8155(H)/8156(H) is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of Port C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Table 1. Table of Port Control Assignment

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{STB}$ (Port A Strobe)	A $\overline{STB}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B $\overline{INTR}$ (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B $\overline{BF}$ (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{STB}$ (Port B Strobe)

Timer Section

The timer is a 14-bit down counter that counts the "timer input" pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register.

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0 – 13 will specify the length of the next count, and bits 14 – 15 will specify the timer output mode. The value loaded into the count length register can have any value from 2_H through $3FFF_H$ in bits 0 – 13.

There are four modes to choose from:

0 – Puts out LOW during second half of count

1 – Square wave

2 – Single pulse upon TC being reached

3 – Repetitive single pulse every time TC is readied and automatic reload of counter upon TC being reached until instructed to stop by a new command loaded into C/S.

Bits 6 – 7 of the Command/Status Register Contents are used to start and stop the counter. There are four commands to choose from. (See the further description on Command/Status Register.)

C/S7	C/S6	
0	0	NOP – Do not affect counter operation.
0	1	STOP – NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC – Stop immediately after present TC is reached (NOP if timer has not started).
1	1	START – Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

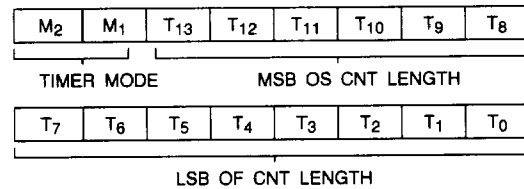
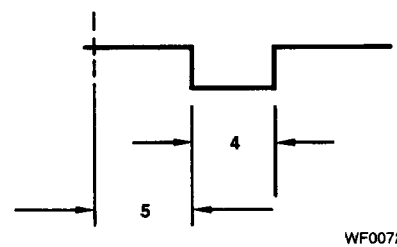


Figure 5. Timer Format

M2 and M1 define the timer mode as follows:

M2	M1	
0	0	Puts out LOW during second half of count.
0	1	Square wave, i.e., the period of the square wave equals the count length programmed with automatic reload at terminal count.
1	0	Single pulse upon TC being reached.
1	1	Automatic reload, i.e., single pulse every time TC is reached.

Note: In case of an asymmetric count, i.e., 9, larger half of the count will be HIGH, the larger count will stay active as shown in Figure 5.



Note: 5 and 4 refer to the number of clock cycles in that time period.

Figure 6. Asymmetric Count

The counter in the 8155(H) is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

8185A Minimum System Configuration

Figure 7 shows a minimum system using three chips, containing 256 Bytes RAM, 2K Bytes EPROM, 38 I/O Pins, 1 Interval Timer, and 4 Interrupt Levels.

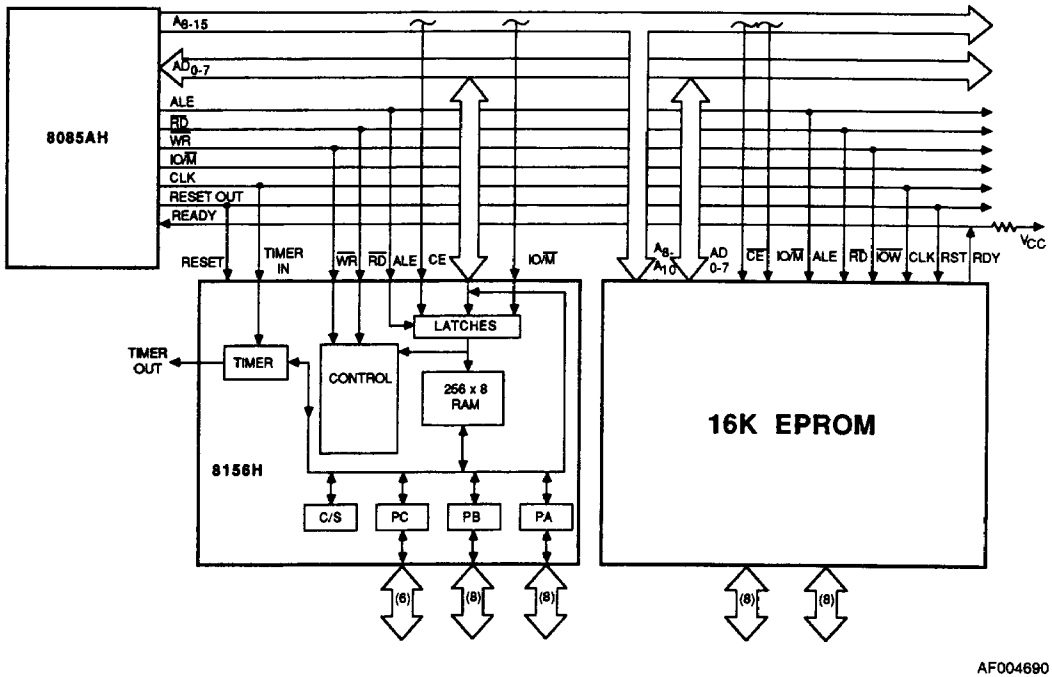


Figure 7. 8085AH Minimum System Configuration (Memory Mapped I/O)

8088 Five-Chip System

Figure 8 shows a five-chip system containing 1.25K Bytes RAM, 2K Bytes EPROM, 38 I/O Pins, 1 Interval Timer, and 2 Interrupt Levels.

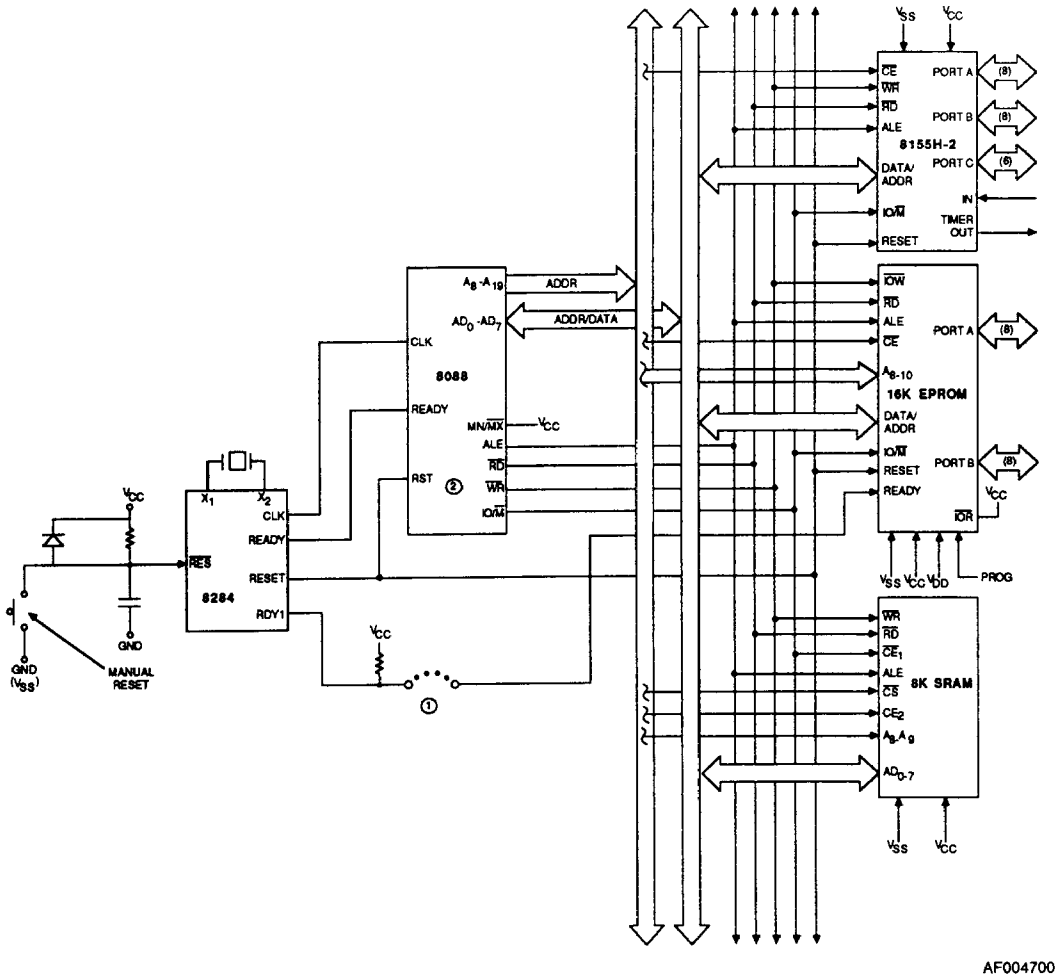


Figure 8. 8088 Five-Chip System Configuration

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
V_{CC} with Respect to V_{SS} ..... −0.5 to +70 V
All Signal Voltages With
Respect to V_{SS} ..... −0.5 V to +7.0 V
Power Dissipation ..... 1.5 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC})
8155/8156 ..... 5 V ±5%
8155H/8156H ..... 5 V ±10%
Supply Current (I_{CC})
8155/8156 ..... 180 mA
8155H/8156H ..... 125 mA

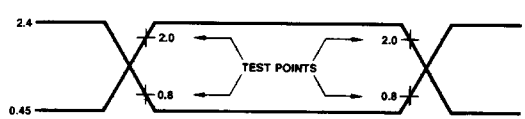
Industrial (I) Devices
Temperature (T_A) ..... −40 to +85°C
Supply Voltage (V_{CC}) ..... 5 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameters	Description		Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage			−0.5	0.8	Volts
V_{IH}	Input High Voltage			2.0	V_{CC}+0.5	Volts
V_{OL}	Output Low Voltage		I_{OL} = 2 mA		0.45	Volts
V_{OH}	Output High Voltage		I_{OH} = −400 µA	2.4		Volts
I_{IL}	Input Leakage		V_{IN} = V_{CC} to 0 V		±10	µA
I_{LO}	Output Leakage Current		0.45 V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	V_{CC} Supply Current	8155, 8156			180	mA
		8155H, 8156H			125	mA
I_{IL} (CE)	Chip Enable Leakage	8155H, 8155	V_{IN} = V_{CC} to 0 V		+100	µA
		8156H, 8156			−100	µA

SWITCHING TEST INPUT/OUTPUT WAVEFORM



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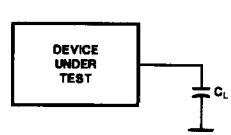
Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Timing measurements are made at 2.0 V for a Logic "1" and 0.8 V for a Logic "0".

SWITCHING TEST CIRCUIT



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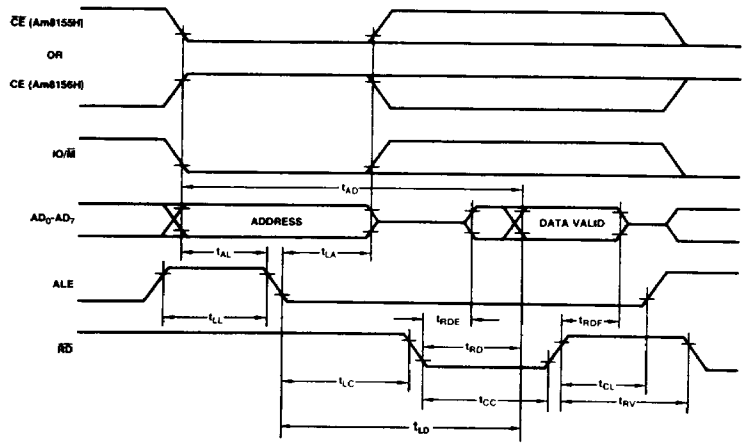
C_L = 150pF
C_L Includes Jig Capacitance

See Section 6 for Thermal Characteristics Information

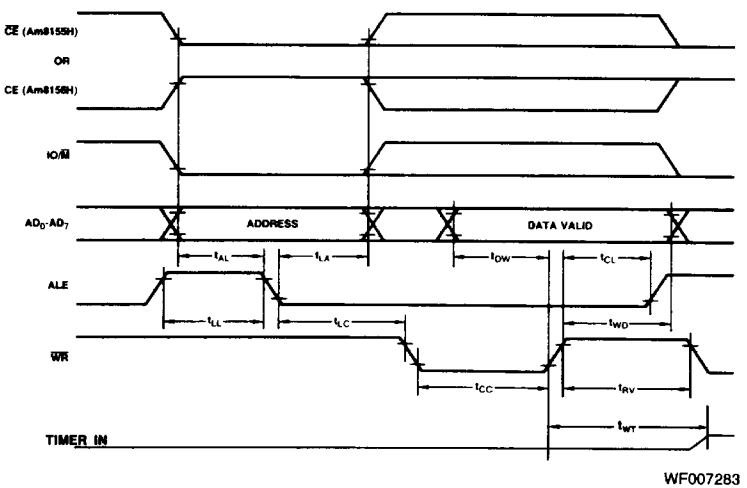
SWITCHING CHARACTERISRICS over operating ranges unless otherwise specified

Parameters	Description	8155, 8156 8155H, 8156H		8155-2, 8156-2 8155H-2, 8156H-2		Units
		Min	Max	Min	Max	
t_{AL}	Address to Latch Setup Time	50		30		ns
t_{LA}	Address Hold Time after Latch	80		30		ns
t_{LC}	Latch to READ/WRITE Control	100		40		ns
t_{RD}	Valid Data Out Delay from READ Control		170		140	ns
t_{AD}	Address Stable to Data Out Valid		400		330	ns
t_{LD}	Latch to Data Out Valed		350		270	ns
t_{WT}	WRITE to TIMER-IN (For Writes Which Start Counting)	360		200		ns
t_{LL}	Latch Enable Width	100		70		ns
t_{RDF}	Data Bus Float After READ	0	100	0	80	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t_{CLL}	WRITE Control to Latch Enable for C/S Register	125		125		ns
t_{CC}	READ/WRITE Control Width	250		200		ns
t_{DW}	Data in to WRITE Setup Time	150		100		ns
t_{WD}	Data in Hold Time After WRITE	25		25		ns
t_{RV}	Recovery Time Between Controls	300		200		ns
t_{WP}	WRITE to Port Output		400		300	ns
t_{PR}	Port Input Setup Time	70		50		ns
t_{RP}	Port Input Hold Time	50		10		ns
t_{SBF}	Strobe to Buffer Full		400		300	ns
t_{SS}	Strobe Width	200		150		ns
t_{RBE}	READ to Buffer Empty		400		300	ns
t_{SI}	Strobe to INTR On		400		300	ns
t_{RDI}	READ to INTR Off		400		300	ns
t_{PSS}	Port Setup Time to Strobe	50		0		ns
t_{PHS}	Port Hold Time After Strobe	120		100		ns
t_{SBE}	Strobe to Buffer Empty		400		300	ns
t_{WBF}	WRITE to Buffer Full		400		300	ns
t_{WI}	WRITE to INTR Off		400		300	ns
t_{TL}	TIMER-IN to TIMER-OUT Low		400		300	ns
t_{TH}	TIMER-IN to TIMER-OUT High		400		300	ns
t_{RDE}	Data Bus Enable from READ Control	10		10		ns
t_1	TIMER-IN Low Time	80		40		ns
t_2	TIMER-IN High Time	120		70		ns

SWITCHING WAVEFORMS

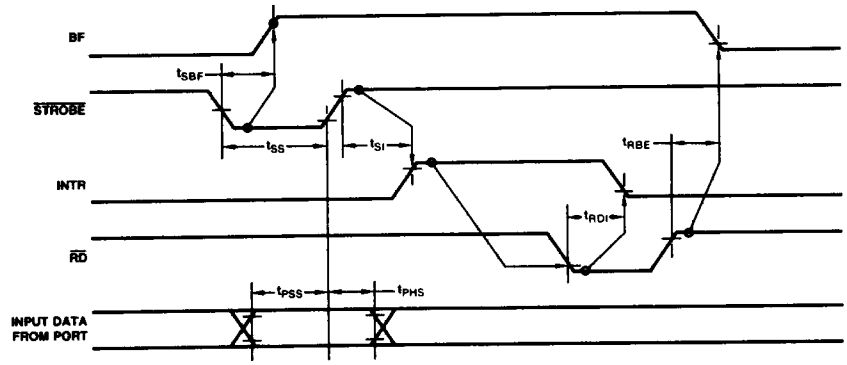


8155(H)/8156(H) Read Cycle

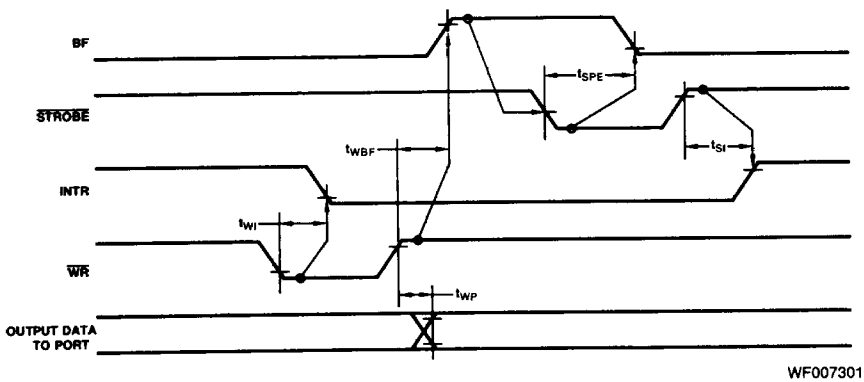


8155(H)/8156(H) Write Cycle

SWITCHING WAVEFORMS (Cont'd.)

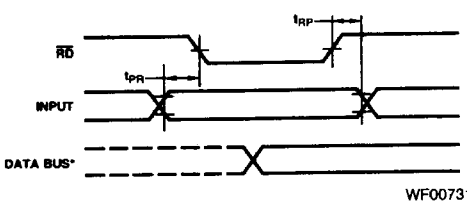


Strobed Input Mode

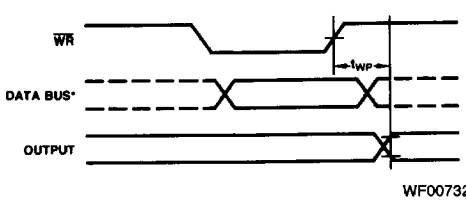


Strobed Output Mode

Input



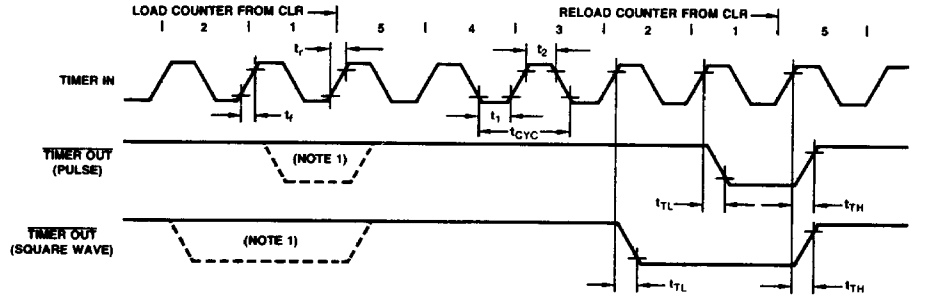
Output



*Data bus timing is shown in Read/Write Cycle diagrams.

Basic I/O Timing Waveform

SWITCHING WAVEFORMS (Cont'd.)



WF007330

Note 1: The timer output is periodic if in an automatic reload mode (M_1 mode bit = 1).

Timer Output Waveform Countdown from 5 to 1