

54AC/74AC157 • 54ACT/74ACT157 Quad 2-Input Multiplexer

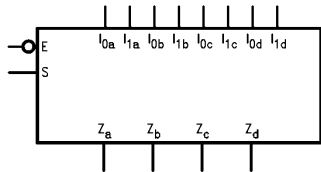
General Description

The 'AC/'ACT157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The 'AC/'ACT157 can also be used as a function generator.

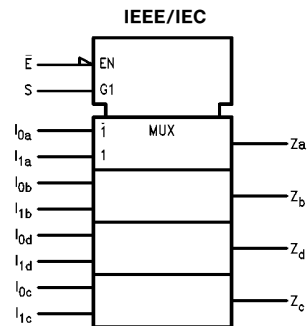
Features

- I_{CC} and I_{OZ} reduced by 50%
- Outputs source/sink 24 mA
- 'ACT157 has TTL-compatible inputs
- Standard Military Drawing (SMD)
 - 'AC157: 5962-89539
 - 'ACT157: 5962-89688

Logic Symbols



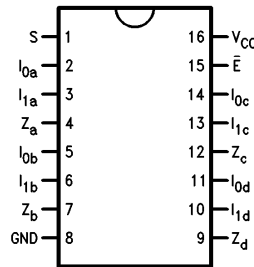
TL/F/9929-1



TL/F/9929-2

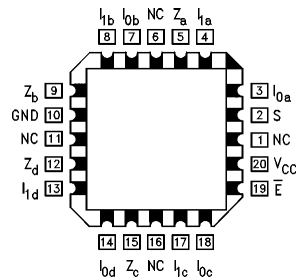
Connection Diagrams

Pin Assignment
for DIP, Flatpak and SOIC



TL/F/9929-3

Pin Assignment
for LCC



TL/F/9929-4

Pin Names	Description
$I_{0a}-I_{0d}$	Source 0 Data Inputs
$I_{1a}-I_{1d}$	Source 1 Data Inputs
\bar{E}	Enable Input
S	Select Input
Z_a-Z_d	Outputs

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Functional Description

The 'AC/ACT157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input (\bar{E}) is active-LOW. When \bar{E} is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The 'AC/ACT157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the 'AC/ACT157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is

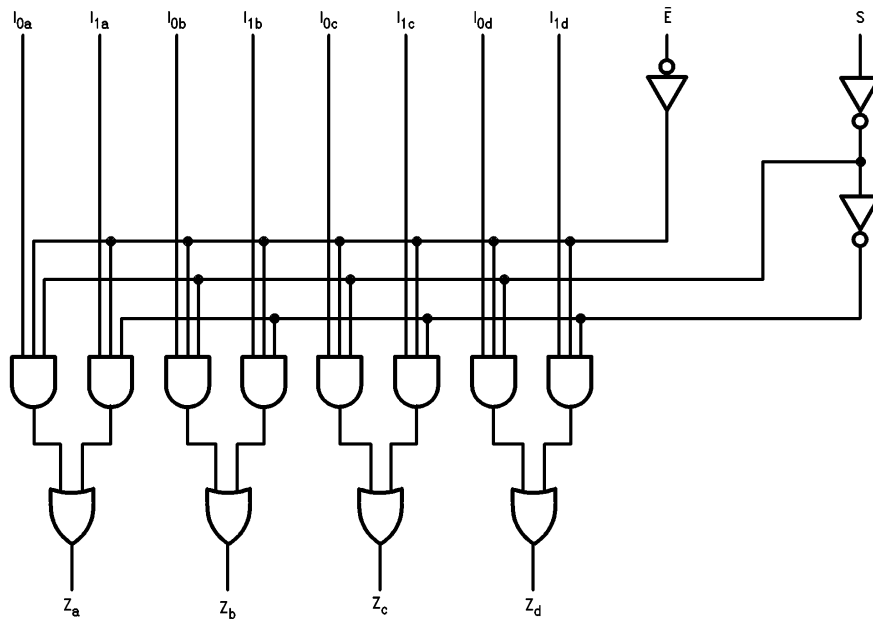
as a function generator. The 'AC/ACT157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

Inputs				Outputs
\bar{E}	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/9929-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	-40°C to +85°C
54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC		54AC	74AC		Units	Conditions
			$T_A = +25^\circ\text{C}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			
			Typ	Guaranteed Limits					
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$
		4.5	4.49	4.4	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4	5.4		
			3.0		2.56	2.4	2.46	V	* $V_{IN} = V_{IL}$ or V_{IH} -12 mA I_{OH} -24 mA -24 mA
			4.5		3.86	3.7	3.76		
			5.5		4.86	4.7	4.76		
			5.5		4.86	4.7	4.76		
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		4.5	0.001	0.1	0.1	0.1			
		5.5	0.001	0.1	0.1	0.1			
			3.0		0.36	0.50	0.44	V	* $V_{IN} = V_{IL}$ or V_{IH} 12 mA I_{OL} 24 mA 24 mA
			4.5		0.36	0.50	0.44		
			5.5		0.36	0.50	0.44		
			5.5		0.36	0.50	0.44		
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}, \text{GND}$	

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74AC		54AC	74AC		Units	Conditions
			T _A = + 25°C		T _A = – 55°C to + 125°C	T _A = – 40°C to + 85°C			
			Typ	Guaranteed Limits					
I _{OLD}	†Minimum Dynamic Output Current	5.5			50		75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			– 50		– 75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0		40.0	μA	V _{IN} = V _{CC} or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	74ACT		54ACT	74ACT		Units	Conditions	
			T _A = + 25°C		T _A = – 55°C to + 125°C	T _A = – 40°C to + 85°C				
			Typ	Guaranteed Limits						
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0		2.0	V	V _{OUT} = 0.1V or V _{CC} – 0.1V	
		5.5	1.5	2.0	2.0		2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8		0.8	V	V _{OUT} = 0.1V or V _{CC} – 0.1V	
		5.5	1.5	0.8	0.8		0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4		4.4	V	I _{OUT} = – 50 μA	
		5.5	5.49	5.4	5.4		5.4			
			4.5		3.86	3.70		3.76	V	*V _{IN} = V _{IL} or V _{IH} – 24 mA – 24 mA
			5.5		4.86	4.70		4.76		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1		0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1		0.1			
			4.5		0.36	0.50		0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA 24 mA
			5.5		0.36	0.50		0.44		
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0		± 1.0	μA	V _I = V _{CC} , GND	
I _{CC} T	Maximum I _{CC} /Input	5.5	0.6		1.6		1.5	mA	V _I = V _{CC} – 2.1V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			50		75	mA	V _{OLD} = 1.65V Max	
I _{OHD}		5.5			– 50		– 75	mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0		40.0	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay S to Z _n	3.3 5.0	1.5 1.5	7.0 5.5	11.5 9.0	1.0 1.0	16.0 12.0	1.5 1.5	13.0 10.0	ns
t _{PHL}	Propagation Delay S to Z _n	3.3 5.0	1.5 1.5	6.5 5.0	11.0 8.5	1.0 1.0	14.0 11.5	1.5 1.0	12.0 9.5	ns
t _{PLH}	Propagation Delay Ē to Z _n	3.3 5.0	1.5 1.5	7.0 5.5	11.5 9.0	1.0 1.0	16.0 12.0	1.5 1.5	13.0 10.0	ns
t _{PHL}	Propagation Delay Ē to Z _n	3.3 5.0	1.5 1.5	6.5 5.5	11.0 9.0	1.0 1.0	14.0 11.5	1.5 1.0	12.0 9.5	ns
t _{PLH}	Propagation Delay I _n to Z _n	3.3 5.0	1.5 1.5	5.0 4.0	8.5 6.5	1.0 1.0	11.0 9.0	1.0 1.0	9.0 7.0	ns
t _{PHL}	Propagation Delay I _n to Z _n	3.3 5.0	1.5 1.5	5.0 4.0	8.0 6.5	1.0 1.0	11.0 9.0	1.0 1.0	9.0 7.0	ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74ACT			54ACT		74ACT		Units
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay S to Z _n	5.0	2.0	5.5	9.0	1.0	11.5	1.5	10.0	ns
t _{PHL}	Propagation Delay S to Z _n	5.0	2.0	5.5	9.5	1.0	11.5	2.0	10.5	ns
t _{PLH}	Propagation Delay Ē to Z _n	5.0	1.5	6.0	10.0	1.0	12.0	1.5	11.5	ns
t _{PHL}	Propagation Delay Ē to Z _n	5.0	1.5	5.0	8.5	1.0	10.0	1.0	9.0	ns
t _{PLH}	Propagation Delay I _n to Z _n	5.0	1.5	4.0	7.0	1.0	8.5	1.0	8.5	ns
t _{PHL}	Propagation Delay I _n to Z _n	5.0	1.5	4.5	7.5	1.0	9.0	1.0	8.5	ns

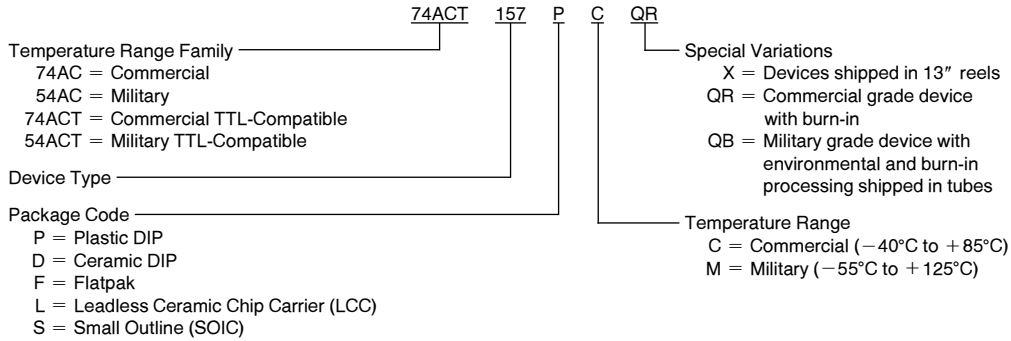
*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

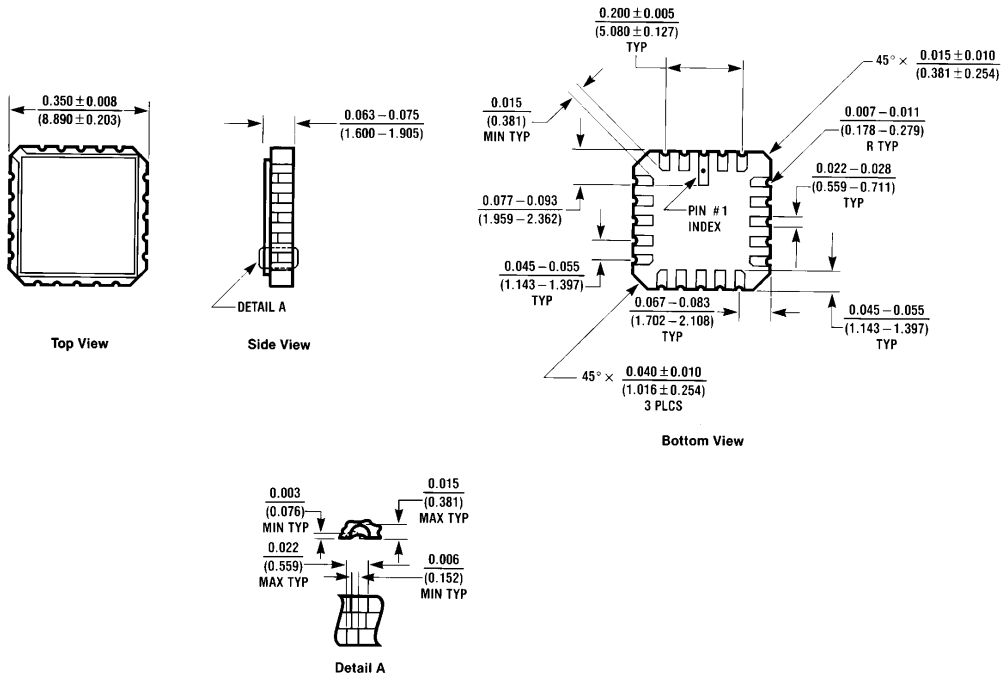
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	50.0	pF	V _{CC} = 5.0V

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



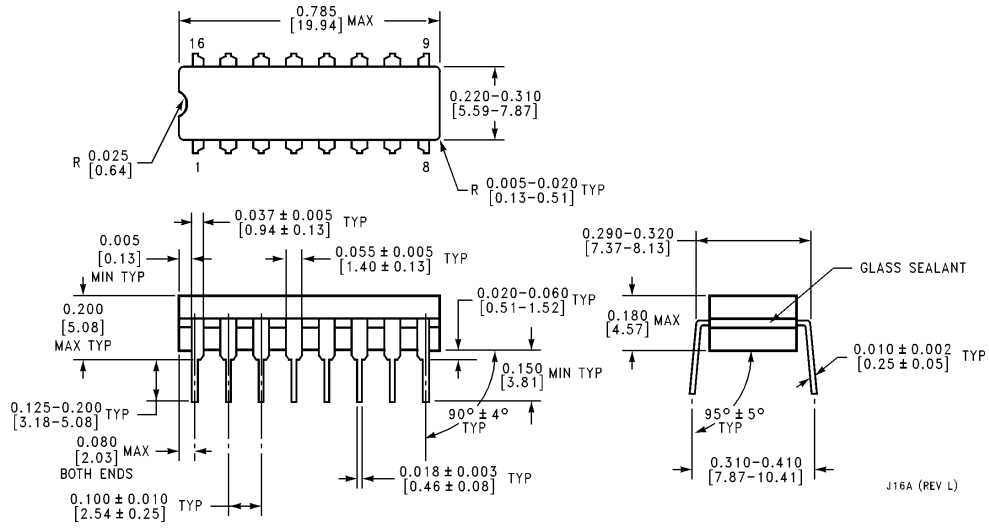
Physical Dimensions inches (millimeters)



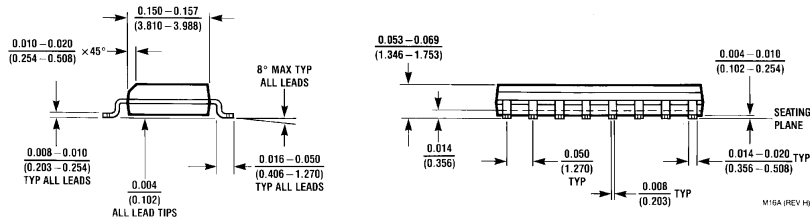
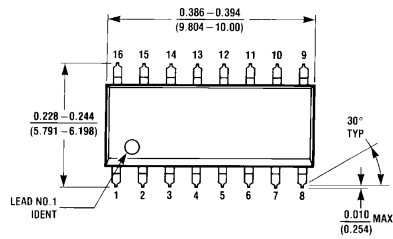
20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)

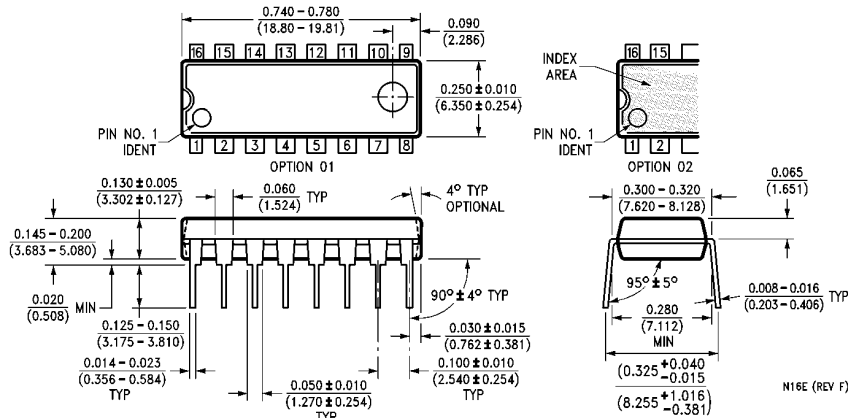


16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

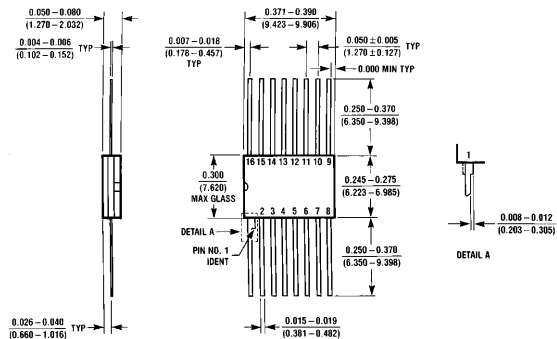


16-Lead Small Outline Integrated Circuit (S)
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Plastic Dual-In-Line Package (P)
NS Package Number N16E



16-Lead Ceramic Flatpak (F)
NS Package Number W16A

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Datasheets for electronics components.

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http://www.ti.com/corp/docs/investor_relations/pr_09_23_2011_national_semiconductor.html

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